LCFC Confidential

EG523 MB Schematics Document

Kabylake-U42 with DDR4 + AMD R17M-M1-70 GPU with GDDR5

2017-03-15

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REV:0.1

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Title	Cover Page	
Size: Custom	Document Number: EG523	Rev: 0.1
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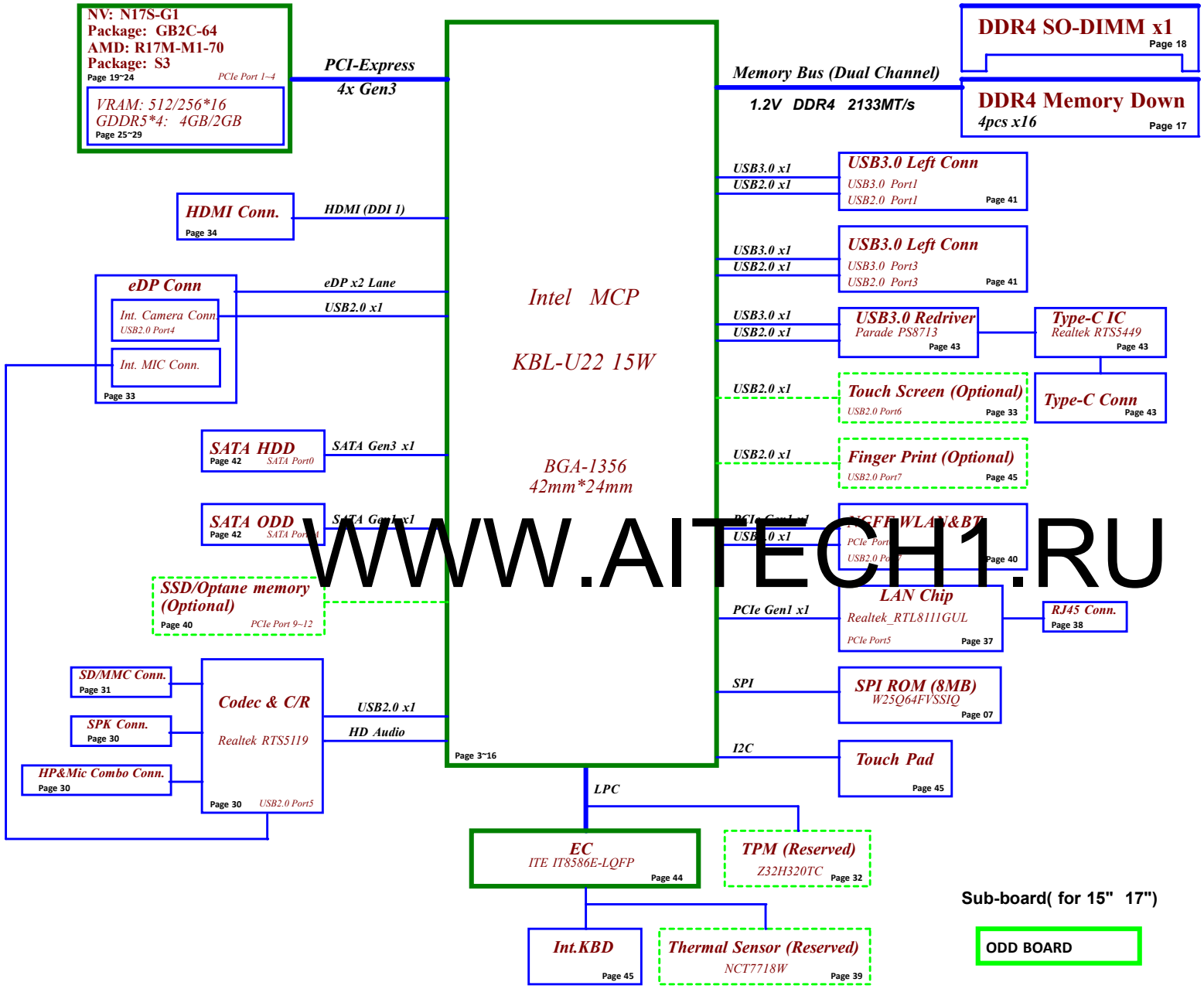

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Title: Block Diagram

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Voltage Rails (O --> Means ON , X --> Means OFF)

State \ Power Plane	V20B+	+3VALW +5VALW +3VALW_PCH +1.8VALW +1.0VALW	+1.2V +2.5V_DDR +VCCST	+5VS +3VS +VCCIO +VCCSTG +VCCSA +VCC_GT +CPU_CORE +0.6VS
S0	O	O	O	O
S3	O	O	O	X
S3 Battery only	O	O	O	X
S5 S4 AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL		SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

HSIO PORT		Function
USB3.0	1	USB3.0 Conn Left
	2	USB Type-C
	3	USB3.0 Conn Left
	4	NC
	5	NC
	6	NC
USB2.0	1	USB3.0 Conn Left
	2	USB Type-C
	3	USB3.0 Conn Left
	4	Finger Print
	5	Cardreader
	6	Touch Panel
	7	Bluetooth
	8	Camera
	9	NC
	10	NC
PCIE	1~4	GPU
	4	CIE
	5	AN
	6	WLAN
	7	SATA HDD
	8	SATA ODD
	9~12 X4 PCIE	Optane Memory
SATA	0	HDD
	1A	ODD
	1B	used as PCIE
	2	used as PCIE

BOM Structure	BTO Item
@	Not stuff
14@	For 14" part
15@	For 15" part
14or15@	For 14" or 15" part
14or17@	For 14" or 17" part
Cannonlake@	For Cannonlake part
CD@	For C cost down
DUALMIC@	For Dual MIC part
EMC@	For EMC part
EMC_15@	For EMC 15" part
EMC_NS@	For EMC nu-stuff part
EMC_PX@	For EMC PX part
EMC_PXNS@	For EMC PX nu-stuff part
ES@	For ES CPU
EXO@	For EXO GPU
ME@	For ME part
NTS@	For nu-touch part
DIS@	For GPU part
OPT@	For NV GPU part
PX@	For AMD GPU part
RANKA@	For VRAM rank A part
RANKB@	For VRAM rank B part
Realtek_SD@	For Realtek SD part
SINGLEMIC@	For single MIC part
SINGLERANK@	For single VRAN rank part
DUALRANK@	For dual VRAN rank part
TS@	For touch screen part
TPM@	For TPM part
UMA@	For UMA part

SMBUS Control Table

	SOURCE	BATT	Charger	DGPU	IT8586E	Memory Down	PCH	PMIC	SODIMM	Thermal Sensor	WLAN WiMAX
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VL_EC	V	V	X	V +3VL_EC	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	X	X	V +3VG_AON	V +3VS	X	V +3VALW_PCH	X	X	V	X
EC_SMB_CK3 EC_SMB_DA3	IT8586E +3VL_EC	X	X	X	V +3VL_EC	X	X	V	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	X	X	V +3VALW_PCH	X	V +3VS	X	V +3VS

EC SMBus1 address

Device	Address
Smart Battery	need to update
Charger	0001 0010 b

EC SMBus2 address

Device	Address
Thermal Sensor(NCT7718W)	1001_100xb
PCH	need to update
DGPU	need to update

EC SMBus3 address

Device	Address
PMIC	need to update

PCH SM Bus address

Device	Address
DDR4 SODIMM	need to update
Wlan	Reserved

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Title: **Notes List**

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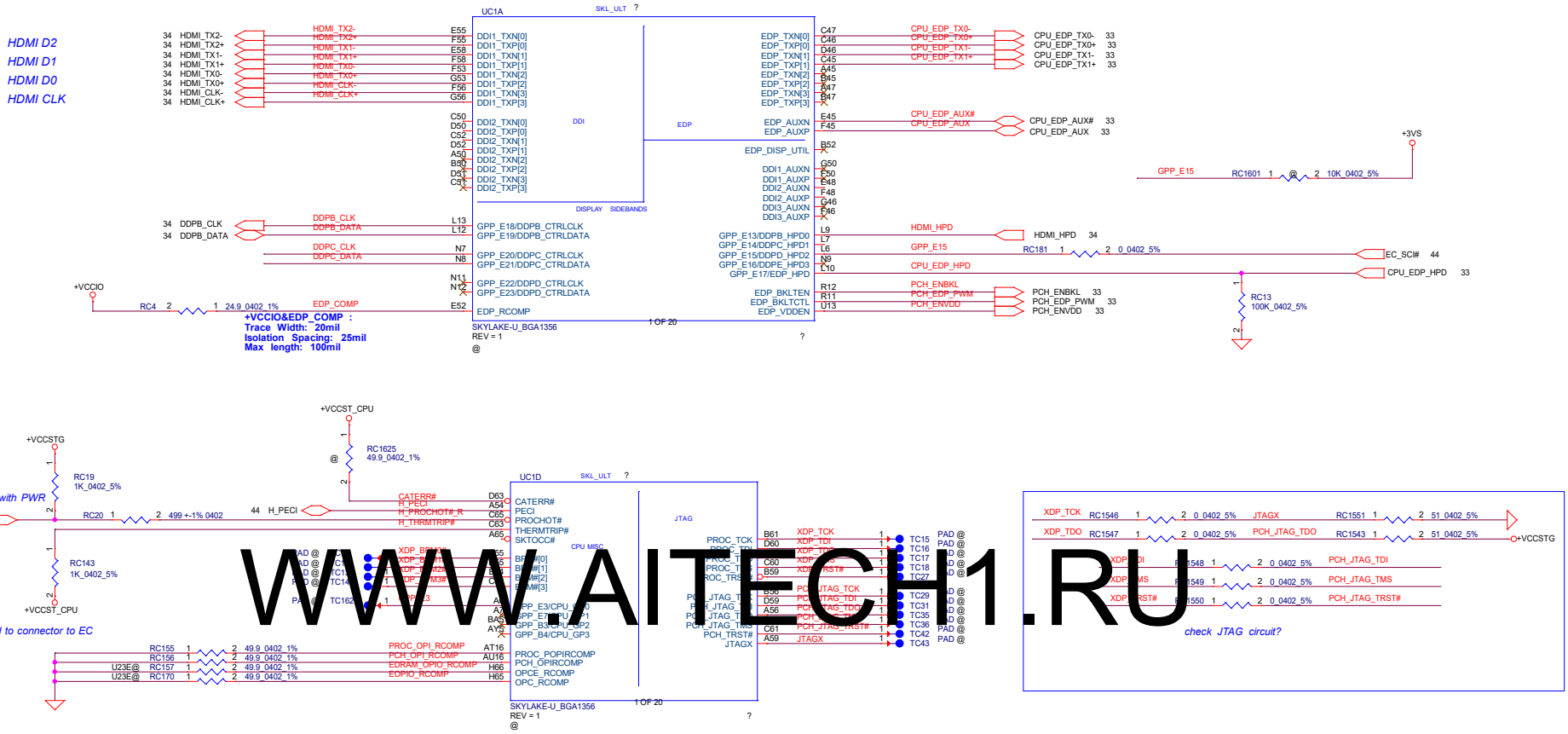

DDP*_CTRLDATA strapping sampled on the rising edge of PWROK

Port	Strap	Enable	Disable
Port 1	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2Kohm	NC
Port 2	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2Kohm	NC

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Title			
MCP (DDI,EDP)			
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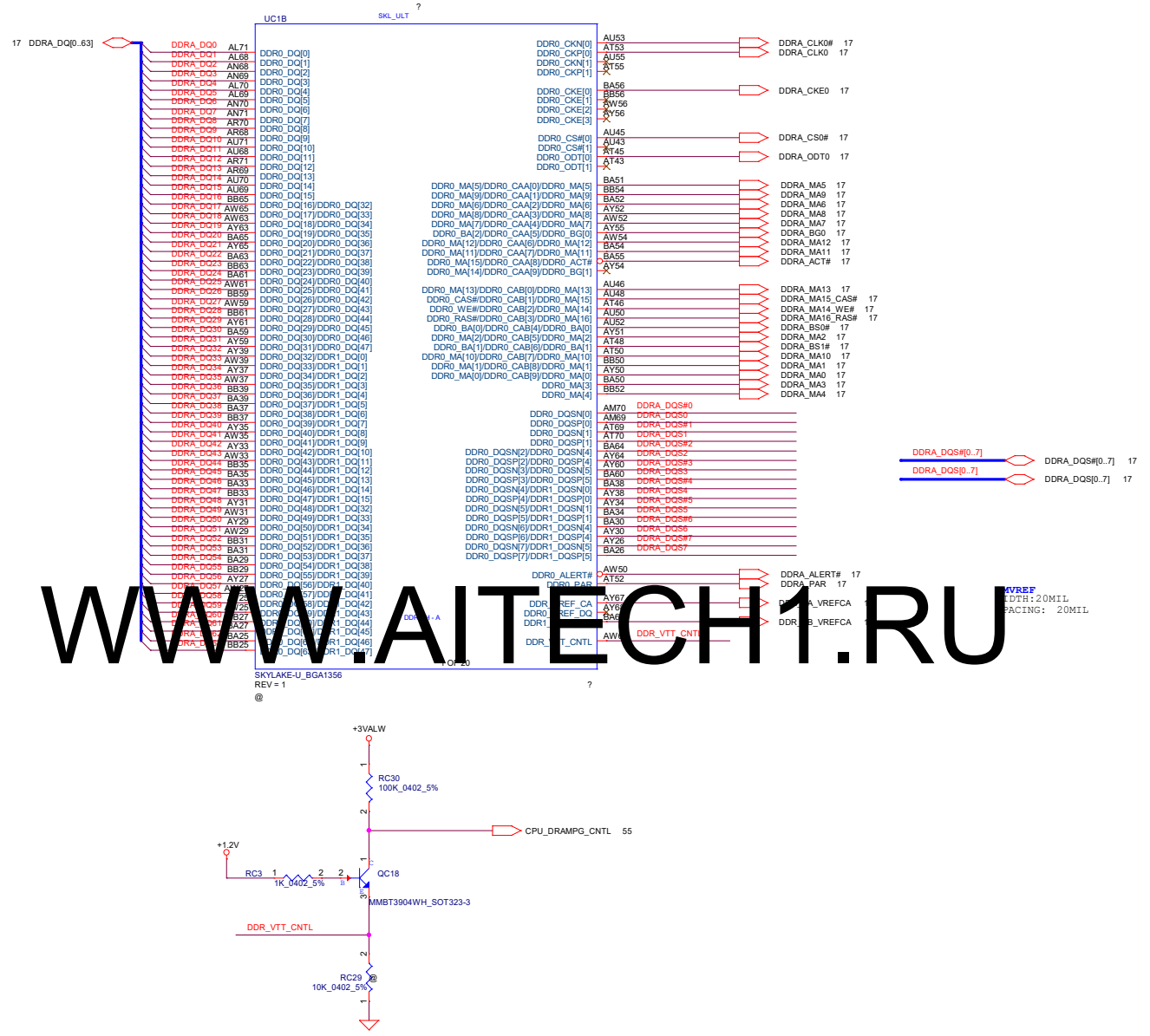

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Title: **MCP (DDR4)**

Size	Document Number	Rev
Custom	EG523	0.1

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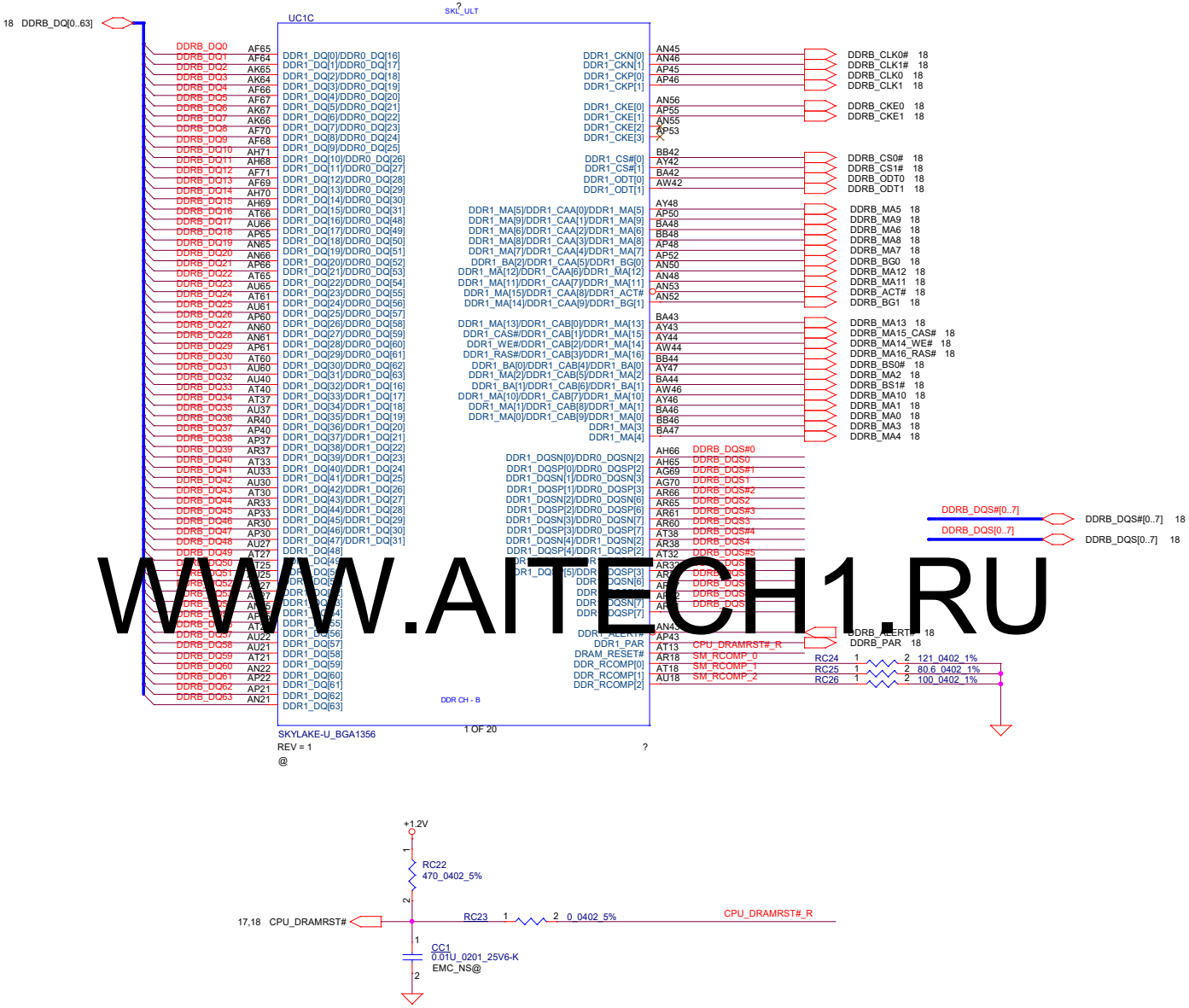

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Title: **MCP (DDR4)**

Size	Document Number	Rev
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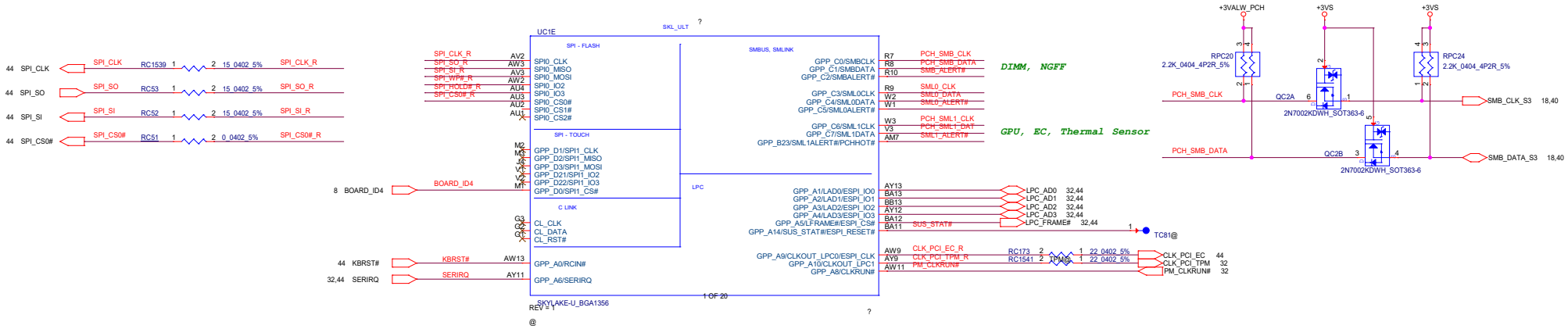

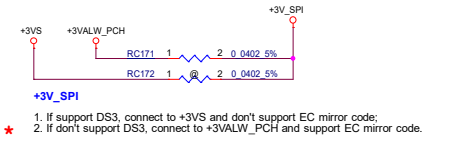

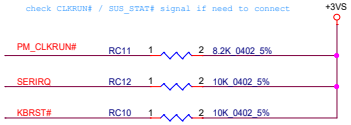

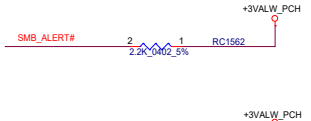

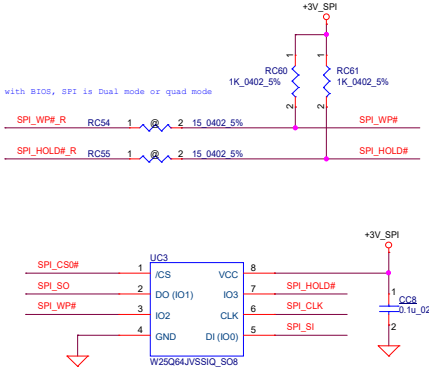

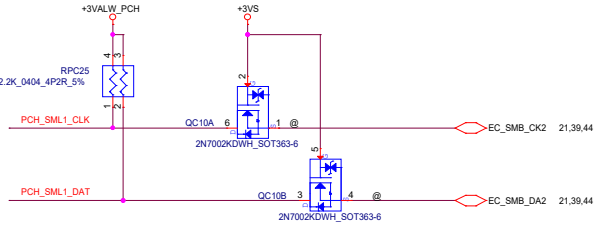

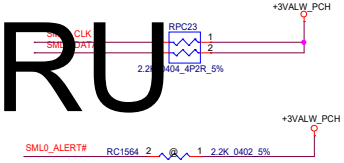

This signal has a weak internal pull-down.
0 = LPC Is selected for EC. (Default)
1 = eSPI Is selected for EC.
Notes:
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary wel
Rising edge of RSMRST#

To enable Direct Connect Interface (DCI), a 150K pull up resistor will need to be added to PCHHOT# pin. This pin must be low during the rising edge of RSMRST#. (Refer to WW52_MOW)

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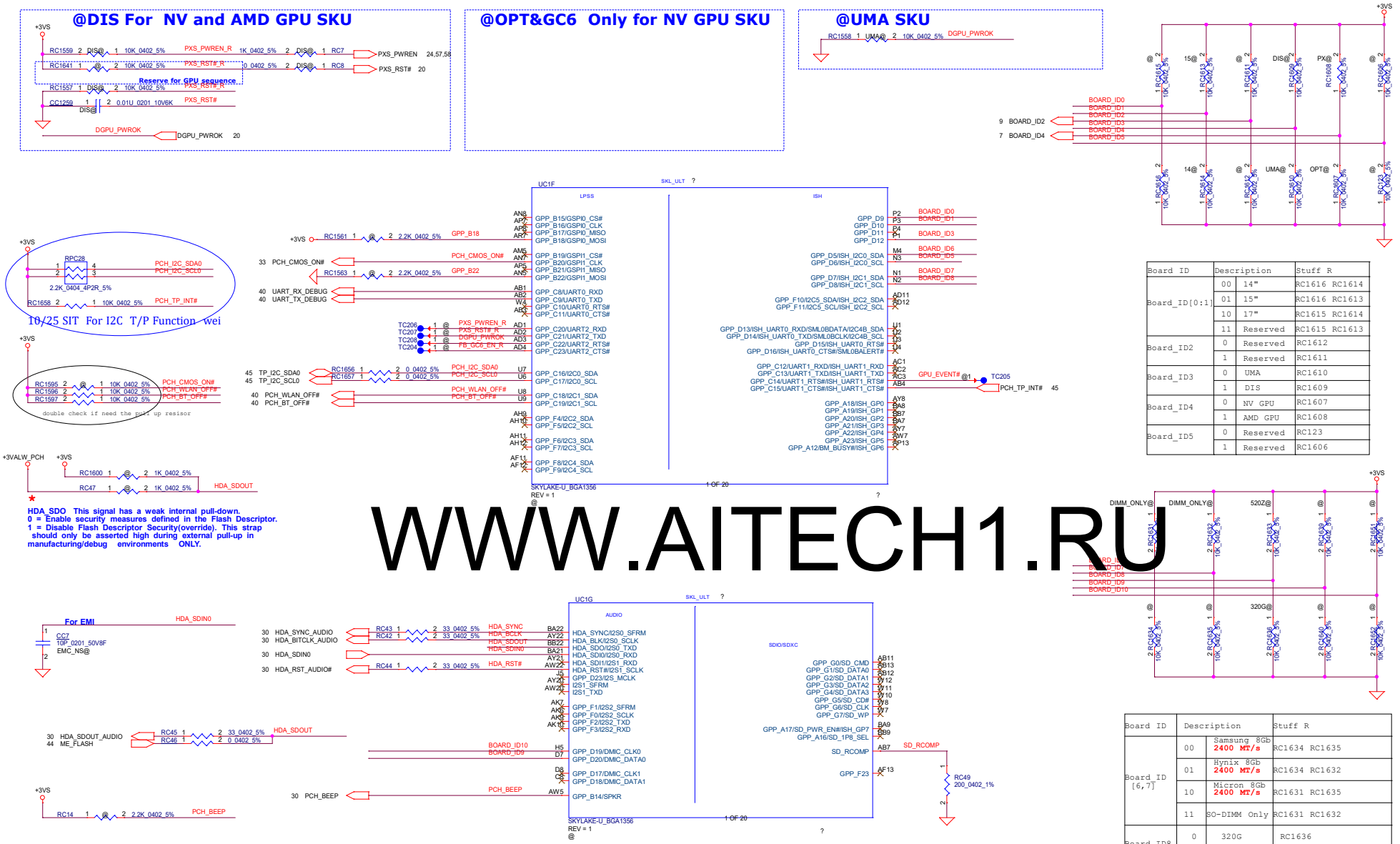
Title	MCP (MISC,JTAG,SPI,LPC,SMB,EC)		
Size C	Document Number EG523		Rev 0.1
Date: Thursday, May 04, 2017	Sheet 7 of 60		



Board ID	Description		Stuff R
Board_ID[0:1]	00	14"	RC1616 RC1614
	01	15"	RC1616 RC1613
	10	17"	RC1615 RC1614
	11	Reserved	RC1615 RC1613
Board_ID2	0	Reserved	RC1612
	1	Reserved	RC1611
Board_ID3	0	UMA	RC1610
	1	DIS	RC1609
Board_ID4	0	NV GPU	RC1607
	1	AMD GPU	RC1608
Board_ID5	0	Reserved	RC123
	1	Reserved	RC1606

Board ID	Description		Stuff R
Board_ID [6,7]	00	Samsung 8Gb 2400 MT/s	RC1634 RC1635
	01	Hynix 8Gb 2400 MT/s	RC1634 RC1632
	10	Micron 8Gb 2400 MT/s	RC1631 RC1635
	11	SO-DIMM Only	RC1631 RC1632
Board_ID8	0	320G	RC1636
	1	520Z	RC1633
Board_ID9	0	Reserved	RC1640
	1	Reserved	RC1639
Board_ID10	0	Reserved	RC1652
	1	Reserved	RC1651

Pin Name	Strap Description	Configuration	Default Value	When Sampled
SPKR / GPP_B14	Top Swap Override	Internal PD 0 = Disable " Top Swap" mode. (Default) ★ 1 = Enable " Top Swap" mode.	0	Rising edge of PCH_PWROK
GSPI0_MOSI /GPP_B18	No Reboot	Internal PD 0 = Disable " No Reboot" mode. (Default) ★ 1 = Enable " No Reboot" mode	0	Rising edge of PCH_PWROK
GSPI1_MOSI /GPP_B22	Boot BIOS Strap Bit BBS	Internal PD 0 = SPI (Default) ★ 1 = LPC	0	Rising edge of PCH_PWROK

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Title			
MCP (LPSS,ISH,AUDIO,SDIO			
Size: C	Document Number: EG523		Rev: 0.1
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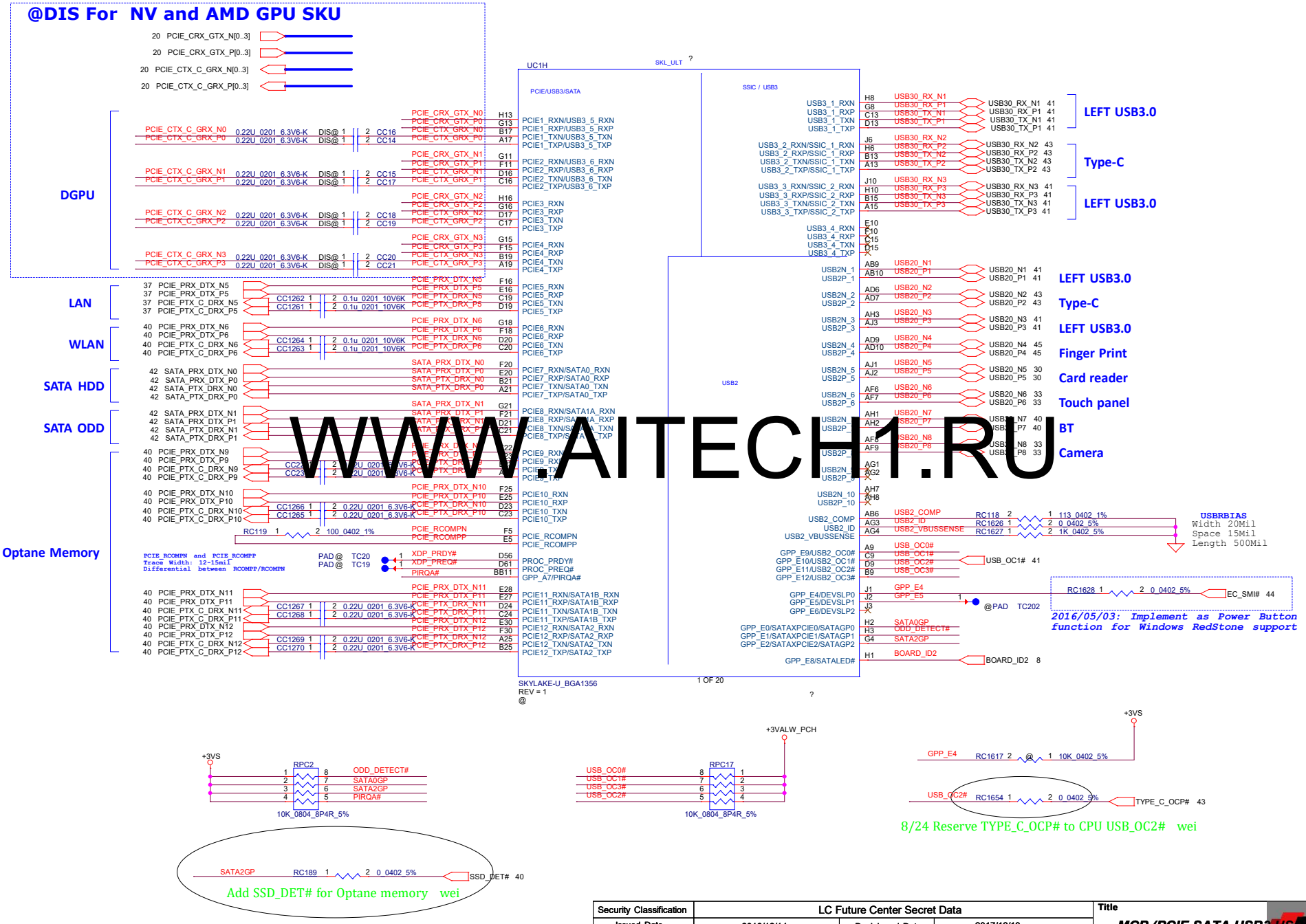

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Title: MCP (PCIE,SATA,USB3,US

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Custom	EG523	0.1

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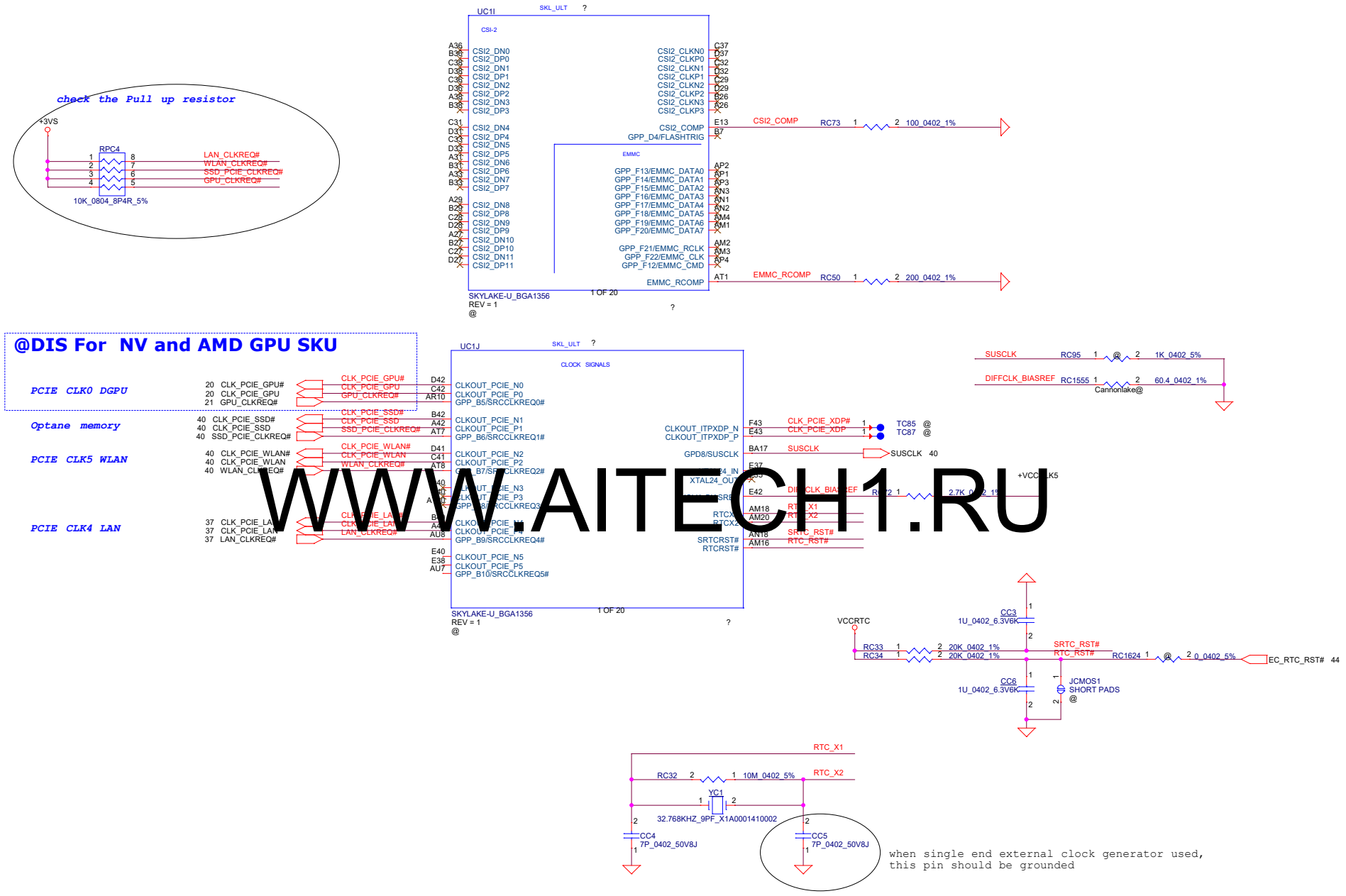

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Title: MCP (CSI2,EMMC,CLOCK)

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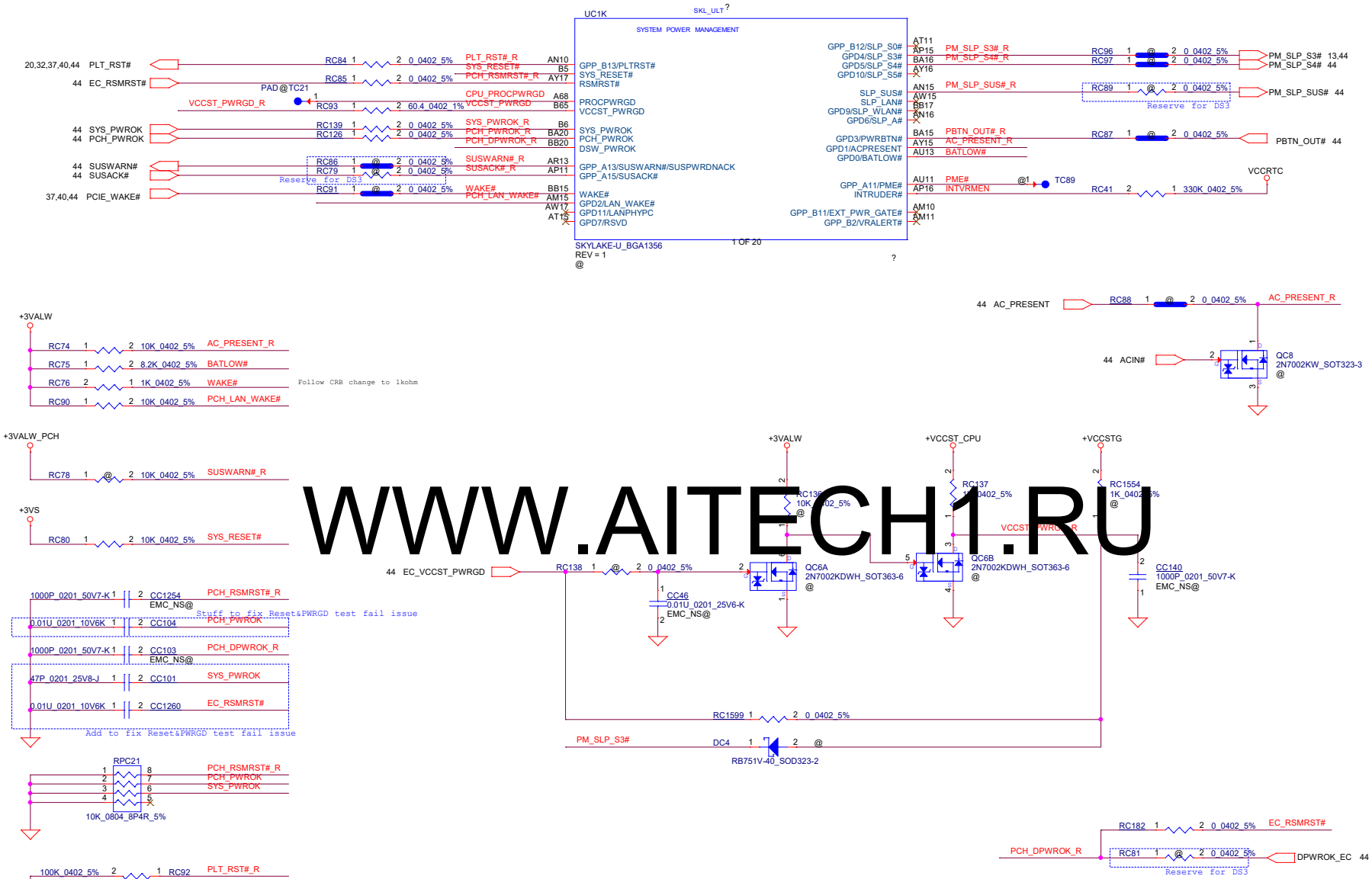

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10/25 SIT Add to fix PLT_RST# glitch issue wei

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Title: MCP (SYSTEM PWR MANAGEMENT)

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Custom	EG523	0.1

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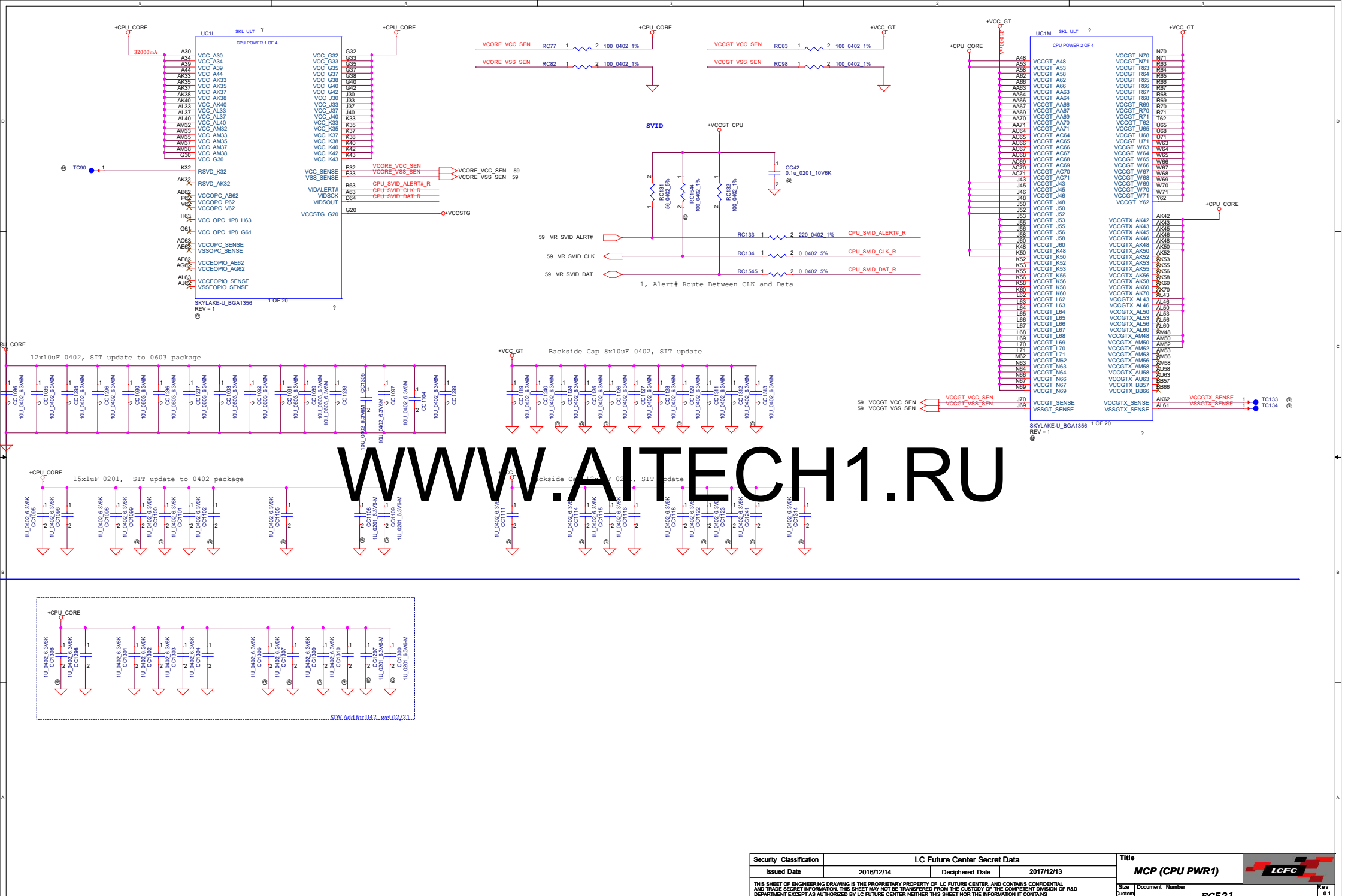

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Title: **MCP (CPU PWR1)**

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Custom	EG521	0.1

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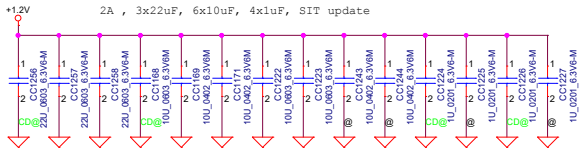

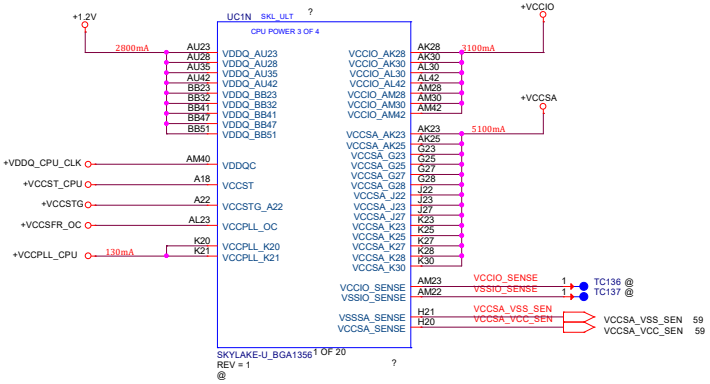

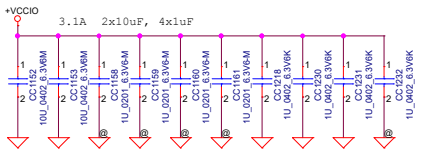

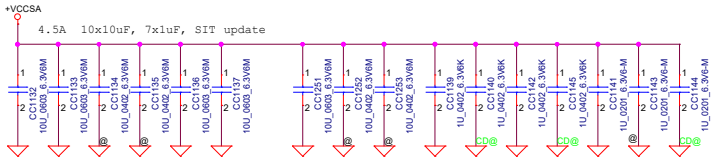

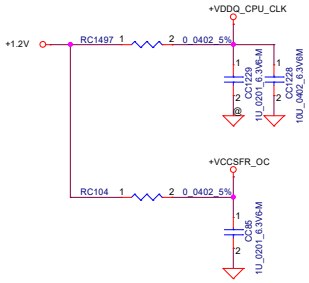

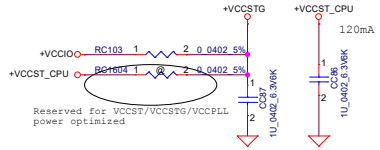

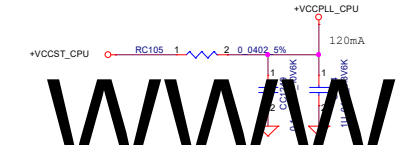

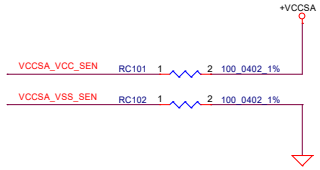

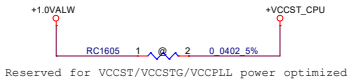

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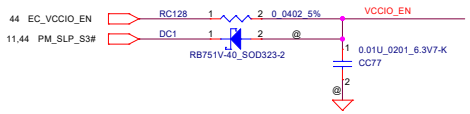

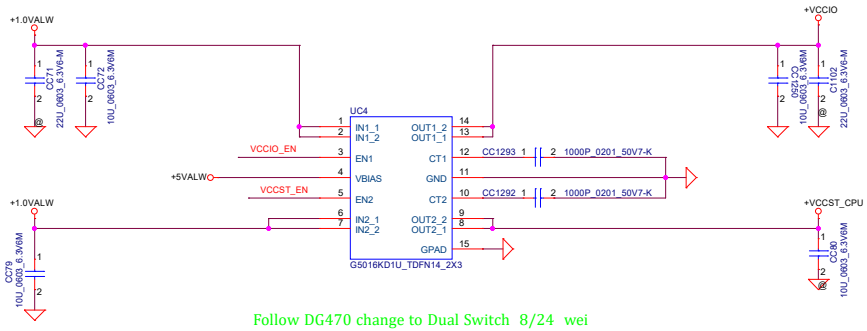

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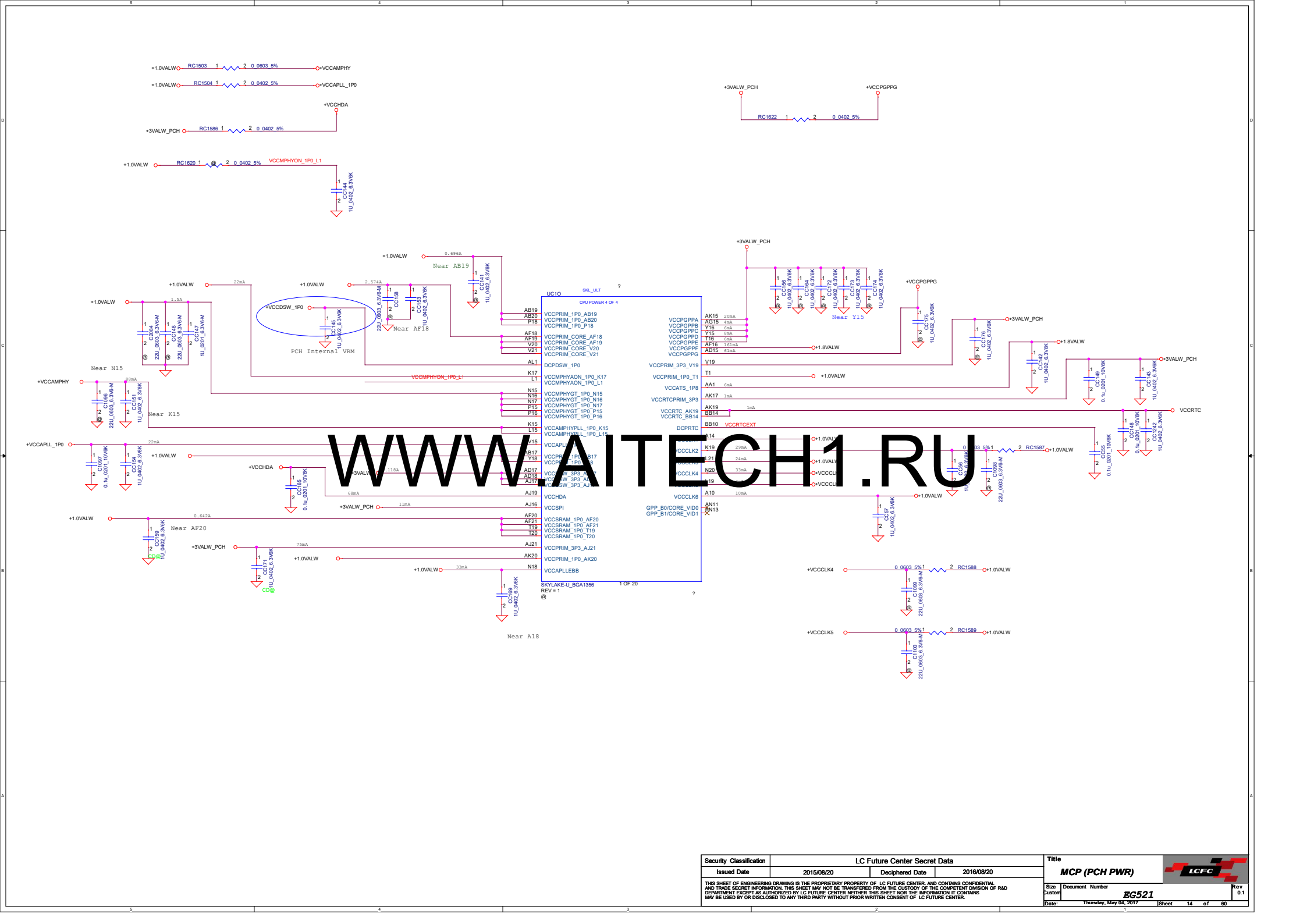
Title: MCP (CPU PWR2)

Size: Custom | Document Number: EG521 | Rev: 0.1

Date: Thursday, May 04, 2017 | Sheet 13 of 60



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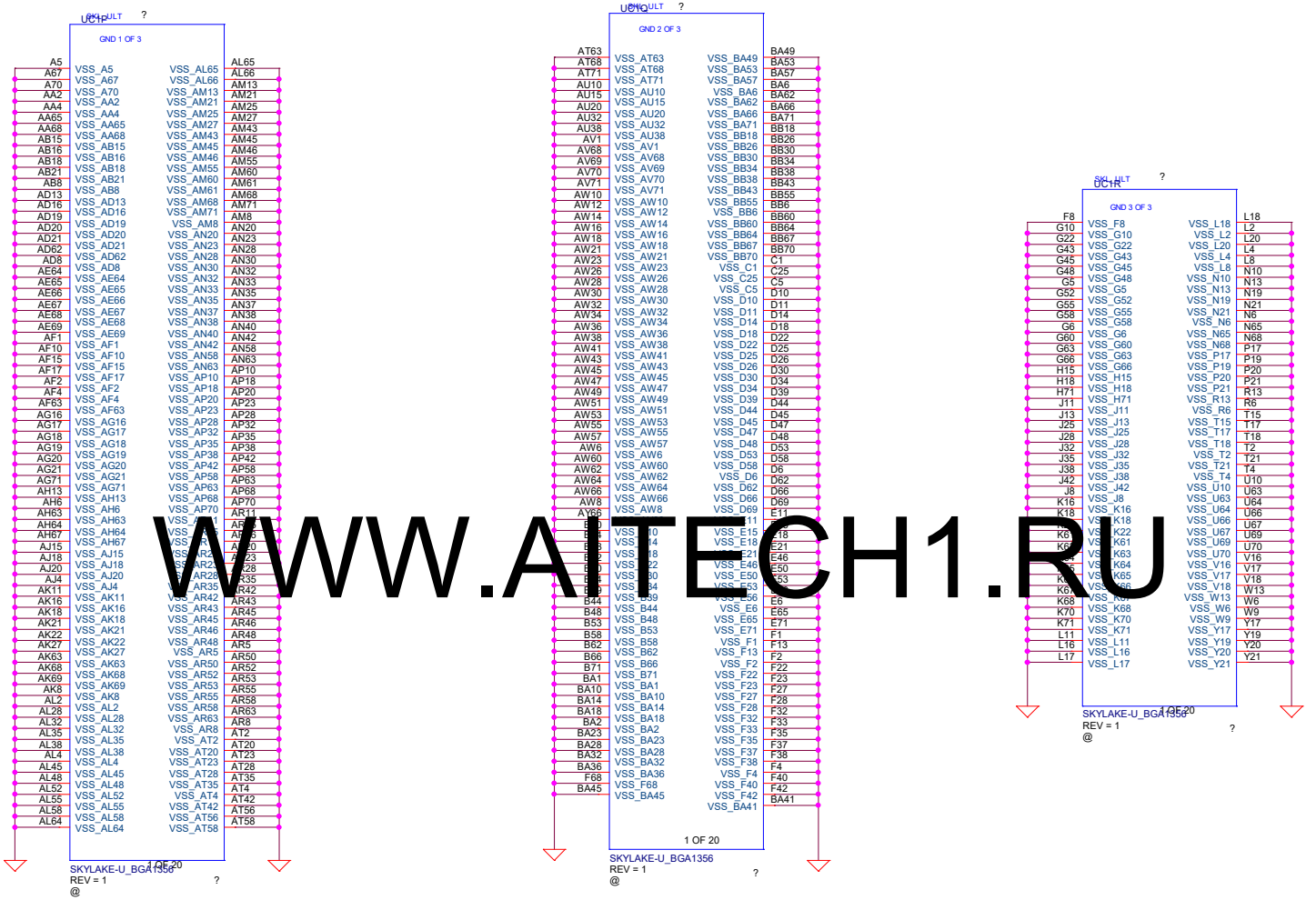
Title: MCP (PCH PWR)

Size: Custom	Document Number: EG521	Rev: 0.1
Date: Thursday, May 04, 2017	Sheet 14 of 60	



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Title: **MCP (VSS)**

Size	Document Number	Rev
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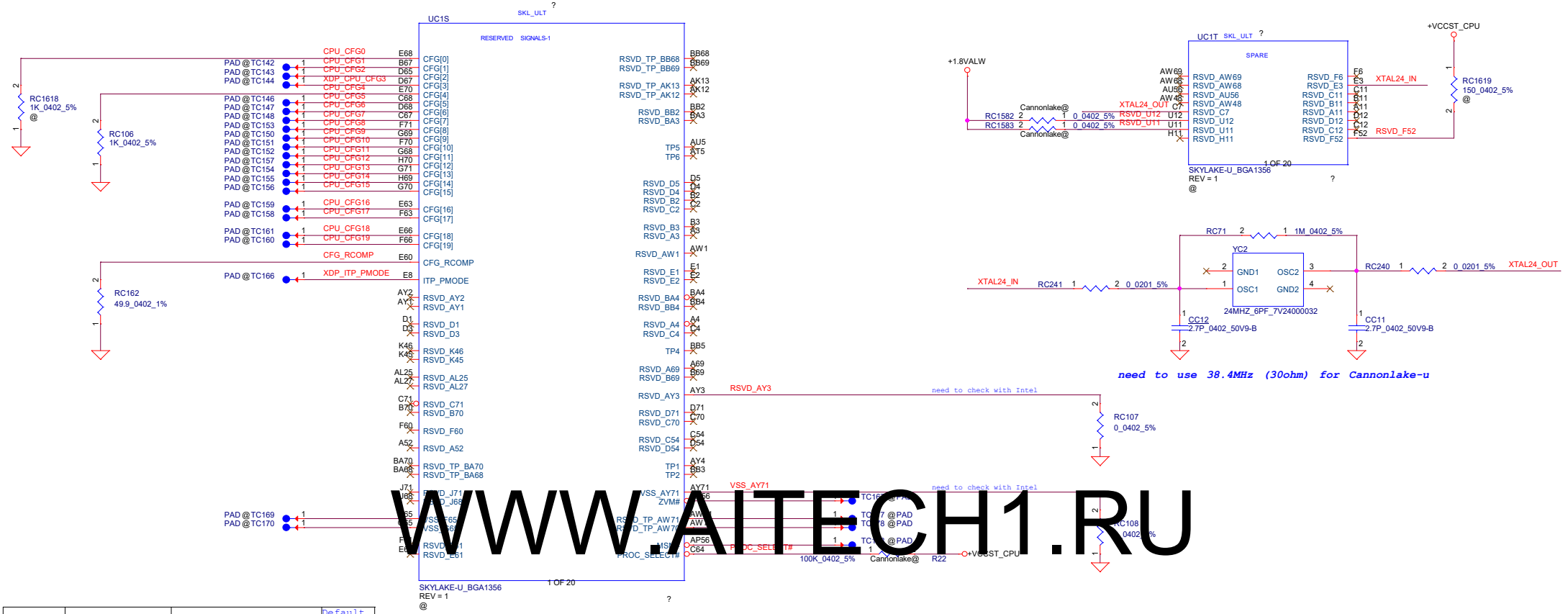
Date: Thursday, May 04, 2017 Sheet 15 of 60



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Pin Name	Strap Description	Configuration	Default Value
CFG[4]	Display Port Presence strap	– 1 = eDP Disabled – 0 = eDP Enabled *	1

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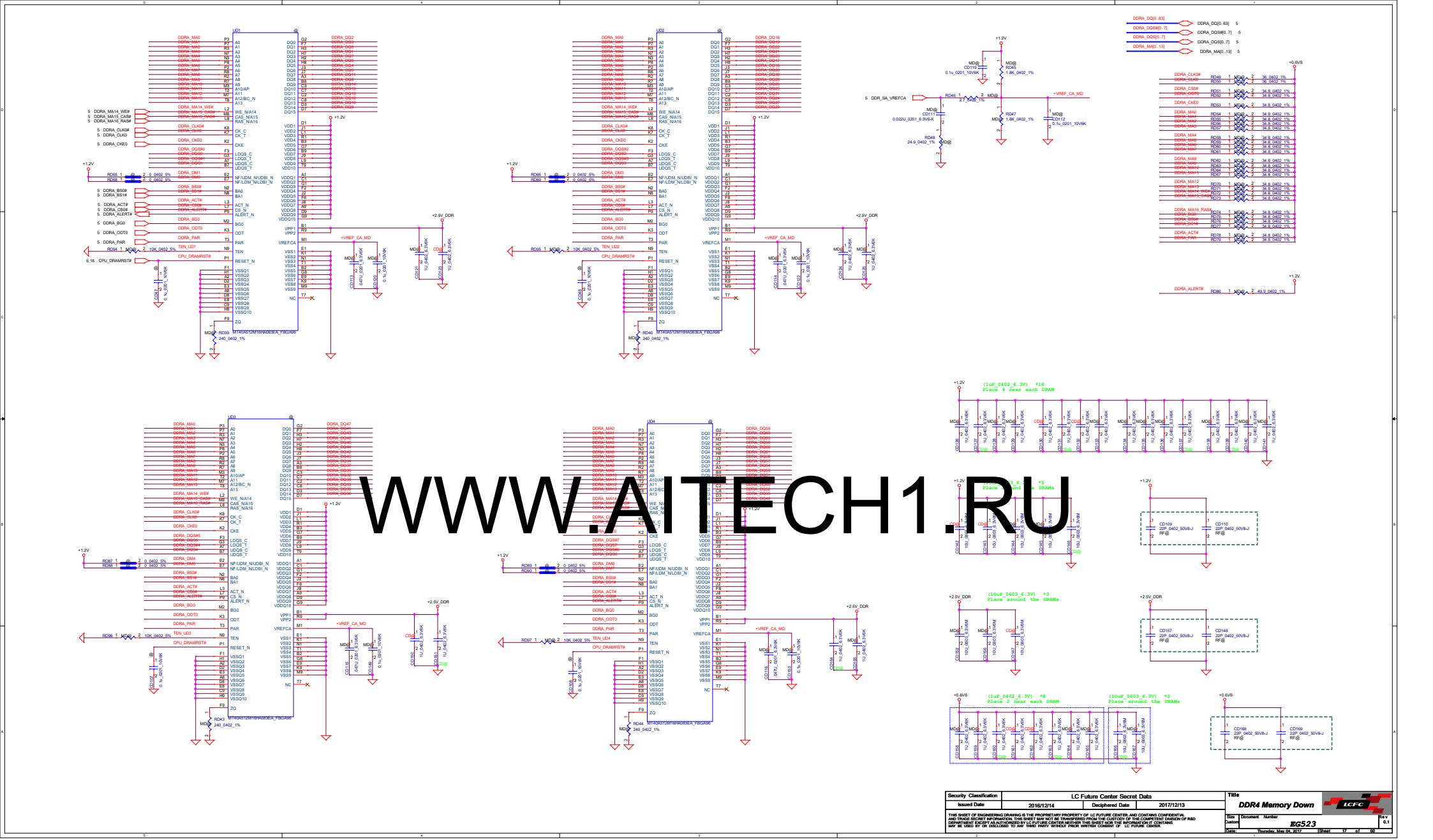
Title: MCP (CFG,RESERVED)

Size	Document Number	Rev
Custom	EG523	0.1

Date: Thursday, May 04, 2017 Sheet 16 of 60



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Title: **DDR4 Memory Down**

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Custom	EG523	0.1

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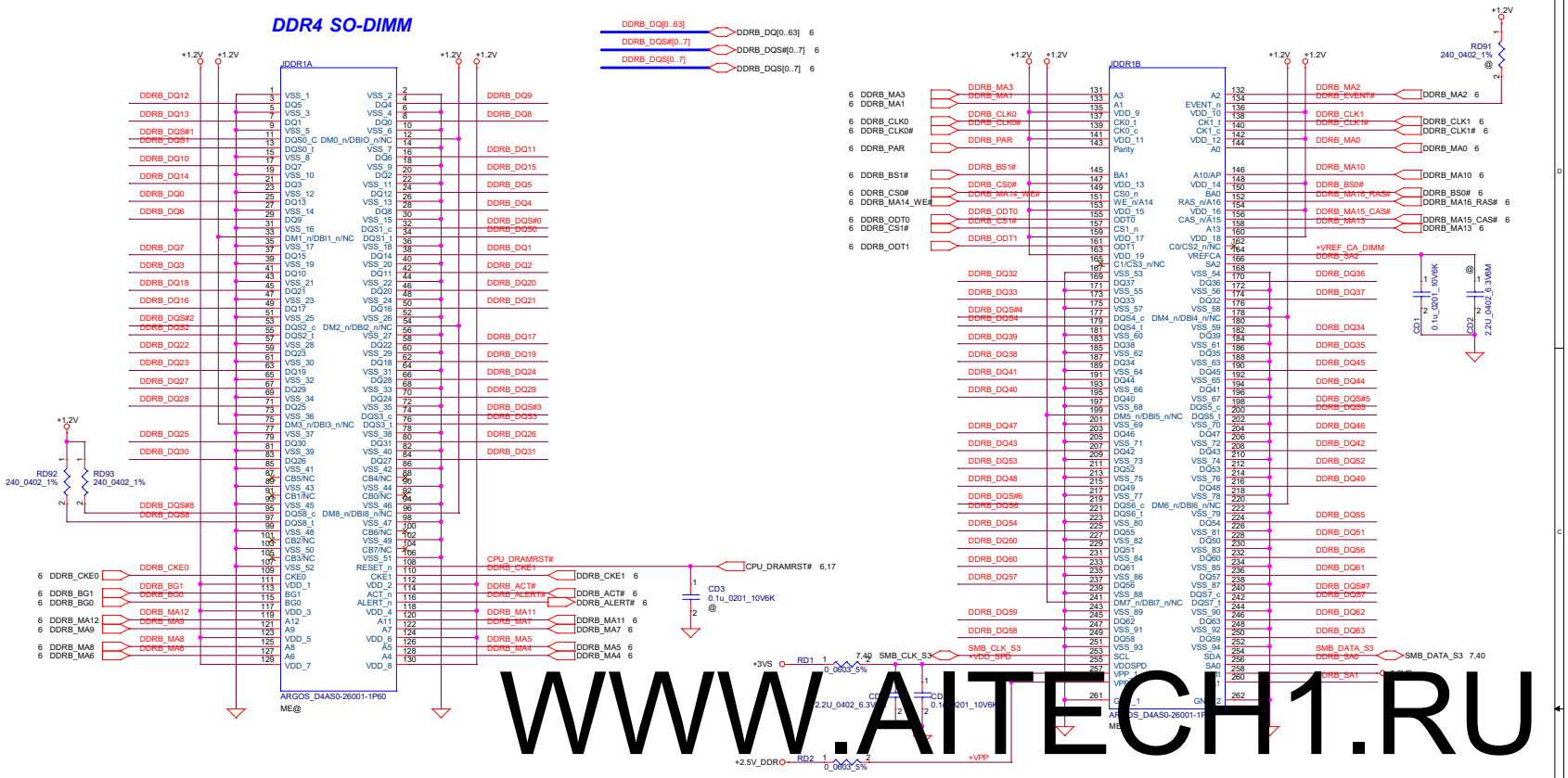
DDR4 SO-DIMM



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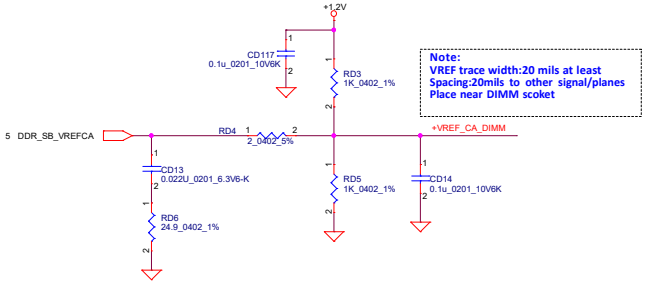
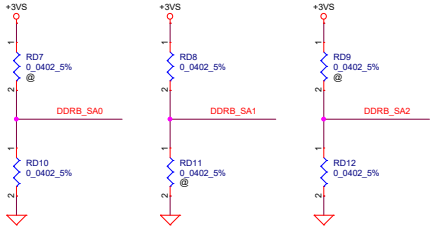
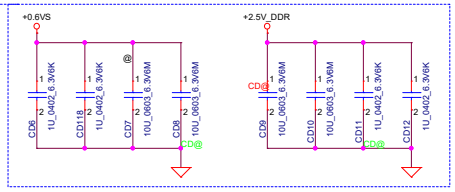
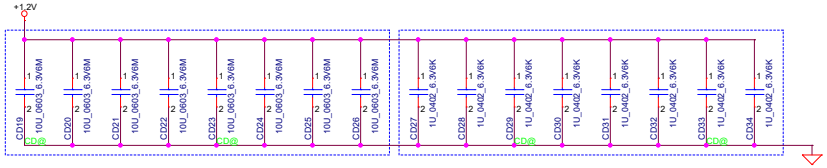
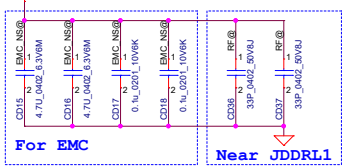




SPD Address = 2H







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Title: DDR4 SO-DIMM

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Power-Up/Down Sequence

"Topaz" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

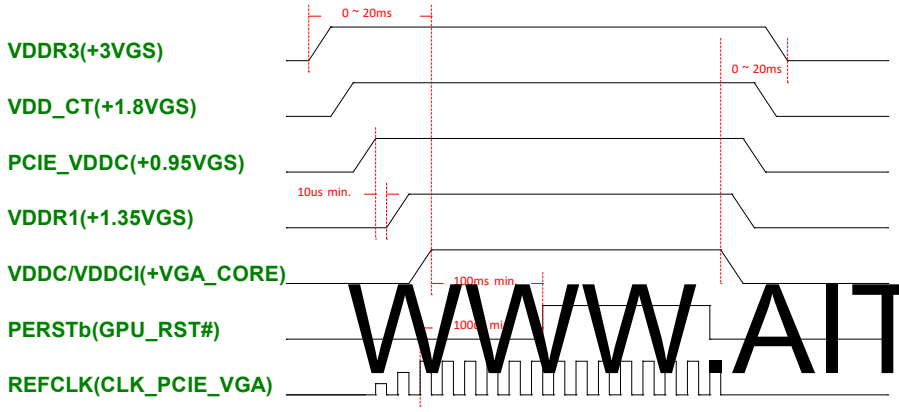
All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µ s.

It is recommended that the 3.3-V rail ramp up first.

The 3.3-V, 1.8-V, and 0.95-V rails must reach their ready state at least 10 µ s before VDDC, VDDCI, and VMEMIO start to ramp up.

The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as ≤ 50 mV/µ s).

For power down, reversing the ramp-up sequence is recommended.



VRAM ID config

Memory Type		VRAM ID PS_3[3:1]	PU resistor RV63	PD resistor RV70
4Gb GDDR5 256M x 16	Hynix H5GC4H24AJR-R0C 6.0Gbps@1.35V	100	4.53K	4.99K
	Micron EDW4032BABG-70-F 6.0Gbps@1.35V	111	4.75K	NC
	Samsung K4G41325FE-HC28 6.0Gbps@1.35V	110	3.4K	10K
8Gb GDDR5 512M x 16	Hynix H5GC8H24MJR-R0C 6.0Gbps@1.35V	000	NC	4.75K
	Micron MT51J256M32HF-70:A 6.0Gbps@1.35V	010	4.53K	2K
	Samsung K4G80325FB-HC28 6.0Gbps@1.35V	001	8.45K	2K

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Title: VGA Notes List

Size	Document Number	Rev
Custom	EG523	0.1

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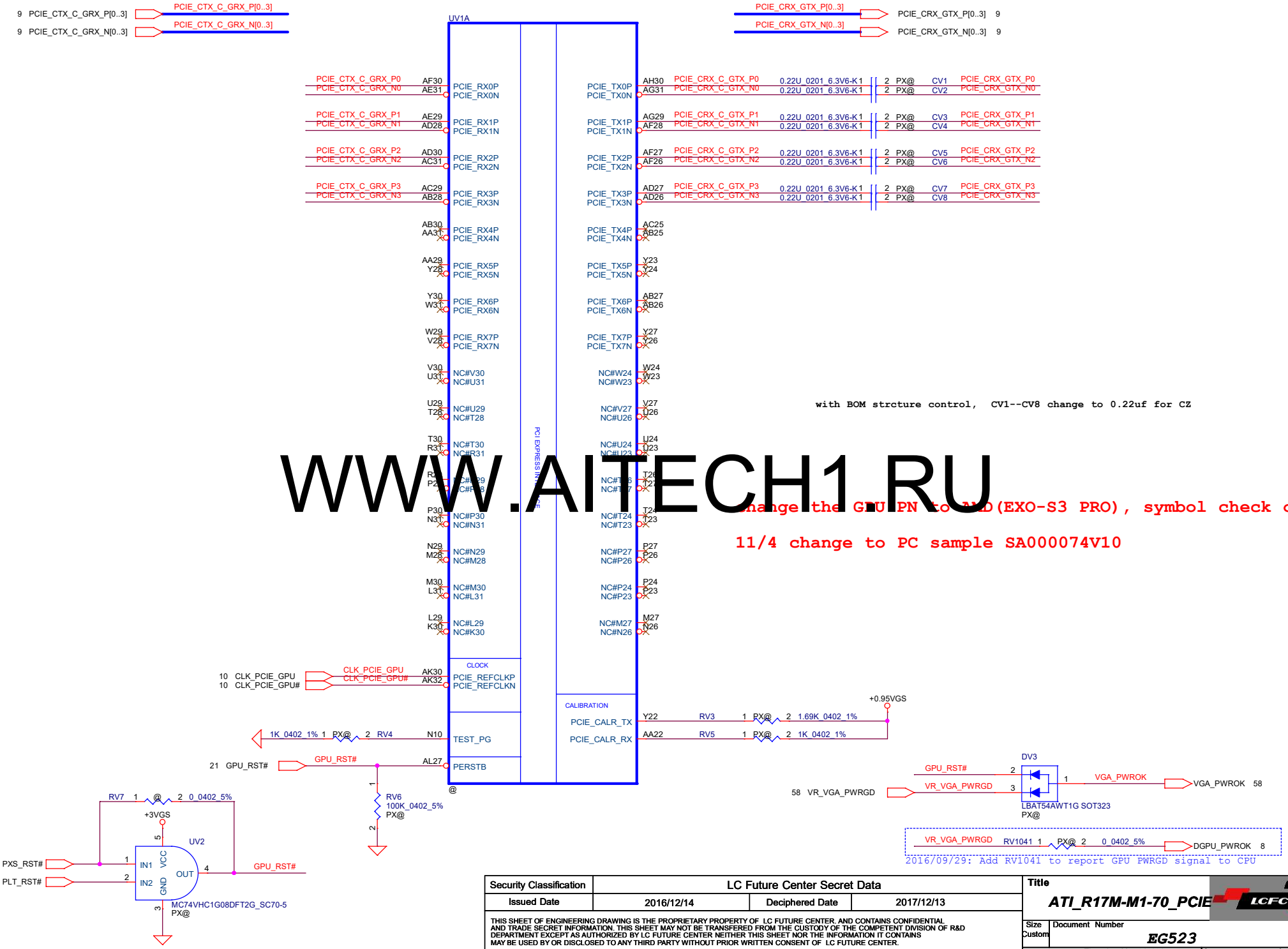

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Title: ATI_R17M-M1-70_PCIE

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CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

MLPS Bit	Strap Name	Description	RECOMMENDED SETTINGS
PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	Define the ROM type when STRAP_BIOS_ROM_EN = 1. Define the primary memory-aperture size when STRAP_BIOS_ROM_EN = 0. 001 = 256MB	x
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	AUD_PORT_CONN_PINSTRAP[0]	The LSB (least significant bit) of the strap option that indicates the number of audio-capable display outputs.	1
PS_1[1]	STRAP_BIF_GEN3_EN_A	1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported. 1= GEN3 is supported	x
PS_1[2]	STRAP_BIF_CLK_PM_EN	0 = The CLKREQB power management capability is disabled 1 = The CLKREQB power management capability is enabled	0
PS_1[3]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled	1
PS_1[5]	STRAP_TX_DEEMPH_EN	0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled. 1= Enable	x
PS_2[1]	N/A	Reserved.	0
PS_2[2]	N/A	Reserved.	0
PS_2[3]	STRAP_BIOS_ROM_EN	0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device. 0= Disable	x
PS_2[4]	STRAP_BIF_VGA_DIS	0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system' s VGA controller.	1
PS_2[5]	N/A	Reserved	1
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	Board configuration related strapping, such as for memory ID 100 = Hynix 4Gb 000 = Hynix 8Gb 111 = Micron 4Gb 010 = Micron 8Gb 110 = Samsung 4Gb 001 = Samsung 8Gb	x
PS_3[4] PS_3[5]	AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[2]	Determines the maximum number of digital display audio endpoints that will be presented to the OS and user.(Combine with PS_0[5]) 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 111= No usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable.	11

PS	PS_3[5:1]	PS_2[5:1]	PS_1[5:1]	PS_0[5]	BOM Option
					R_pu (Ω) / R_pd (Ω) / CV (pF)
PS_0[5]	1	1	0	0	RV71=8.45K RV77=2K CV15=NC
PS_1[5:1]	1	1	0	0	1 RV74=8.45K RV80=2K CV16=NC
PS_2[5:1]	1	1	0	0	0 RV60=NC RV69=4.75K CV18=NC
PS_3[5:1]	1	1	X	X	RV63=X76 RV70=X76 CV19=NC

with BOM strcture control,
RV63,RV70 change to different value to adjust VRAM config

with BOM strcture control,
when config PEG3
RV74 change to 8.45K,
RV80 change to 2K

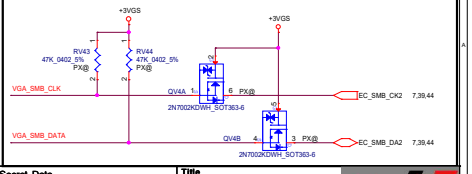
Capacitor Value (nF)	Bits [5:4]
680	00
82	01
10	10
NC	11

R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

SVC	SVD	Output Voltage (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

Internal VGA Thermal Sensor



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Title: ATI_R17M-M1-70_Main_MSIC

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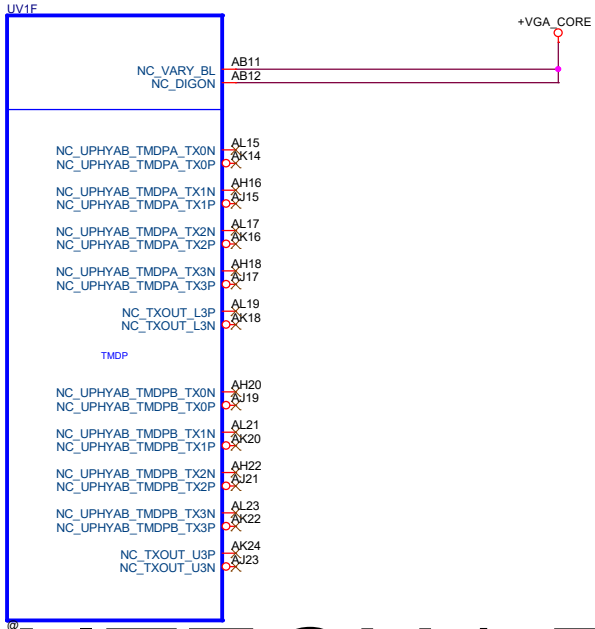

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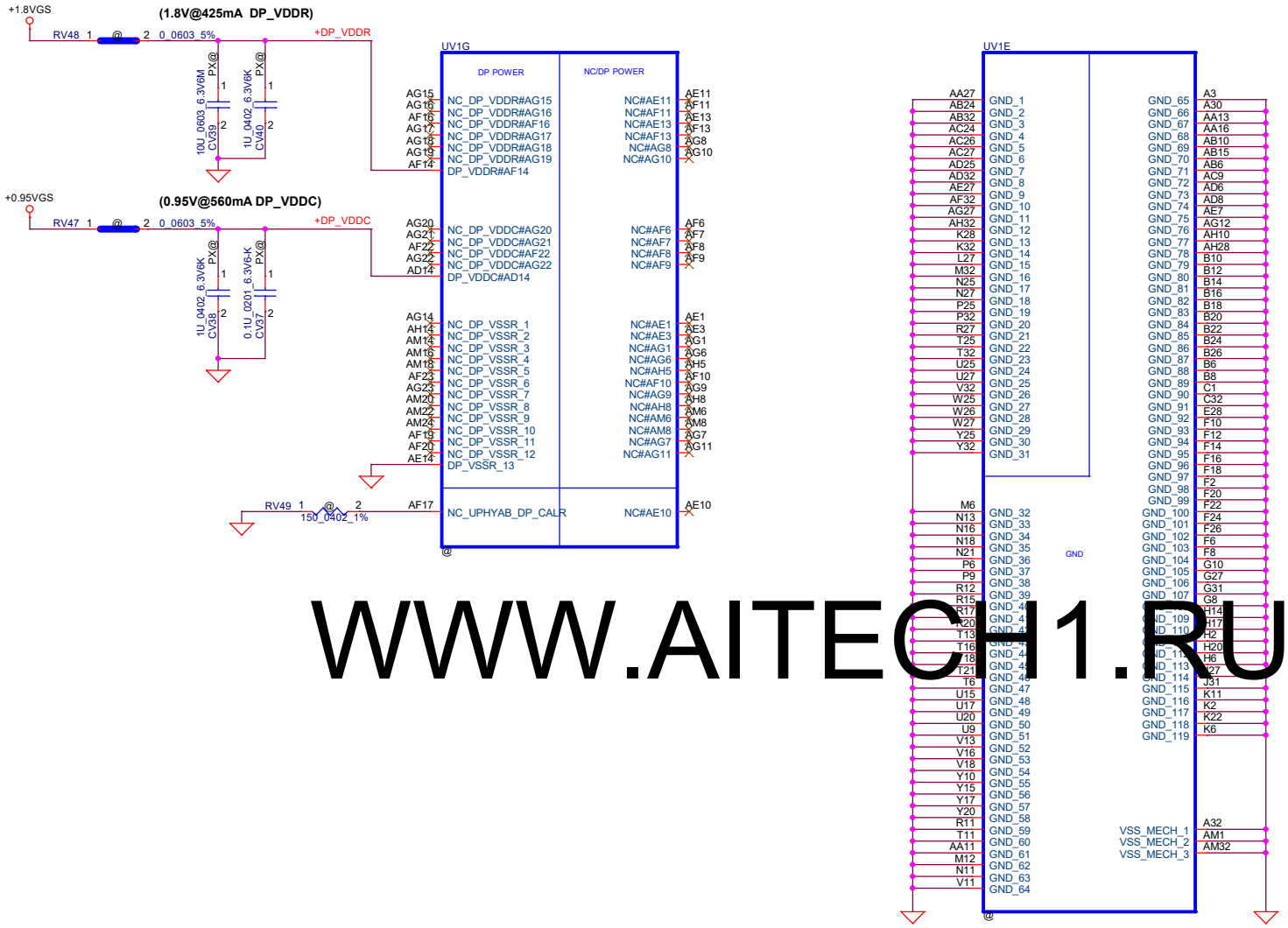
Title: ATI_R17M-M1-70_TMDP

Size: Custom	Document Number: EG523	Rev: 0.1
Date: Thursday, May 04, 2017	Sheet 22 of 60	



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Title: ATI_R17M-M1-70_DP Powe

Size	Document Number	Rev
Custom	EG523	0.1

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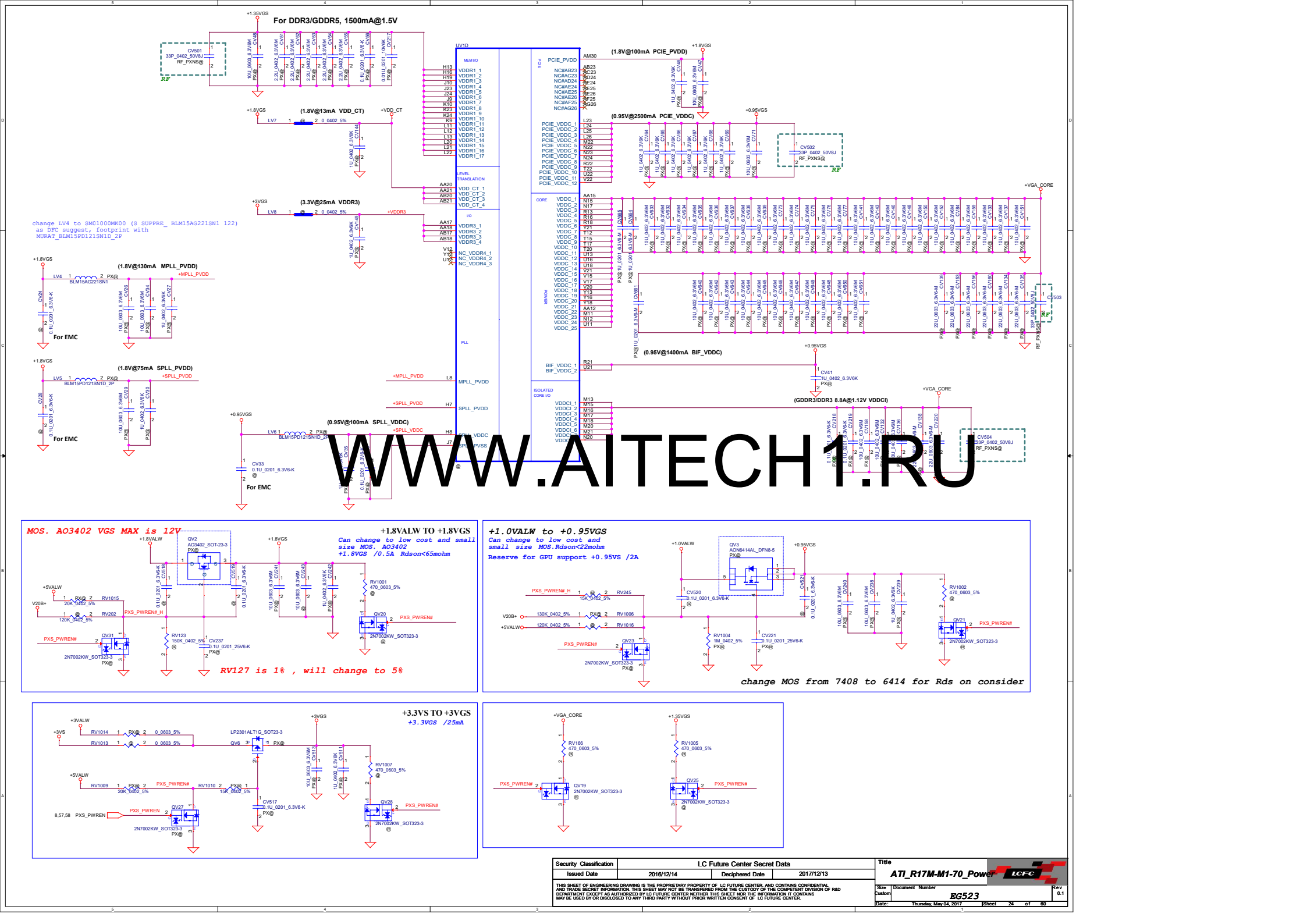

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Title: ATI_R17M-M1-70_Power

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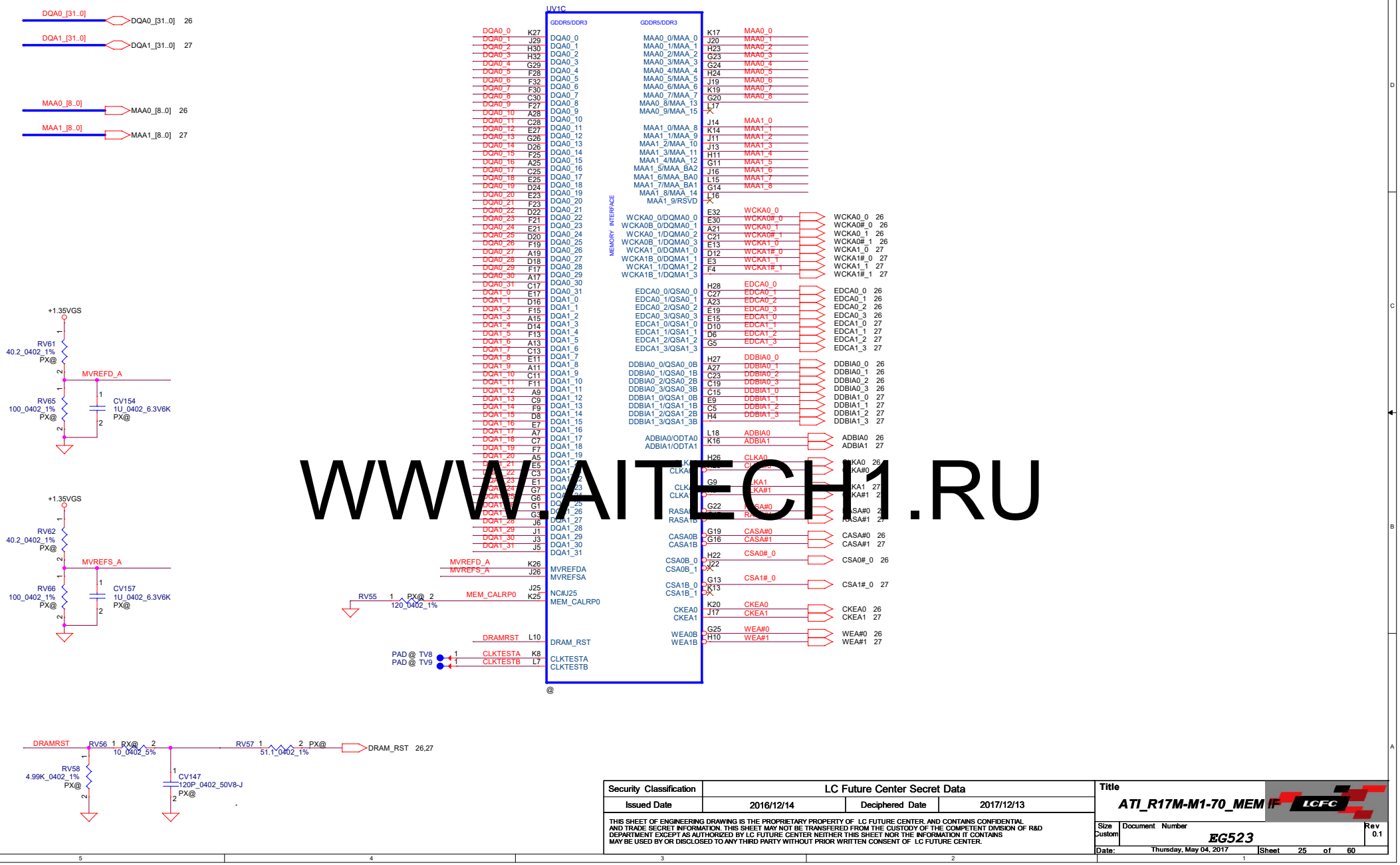

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Title: ATI_R17M-M1-70_MEM IF

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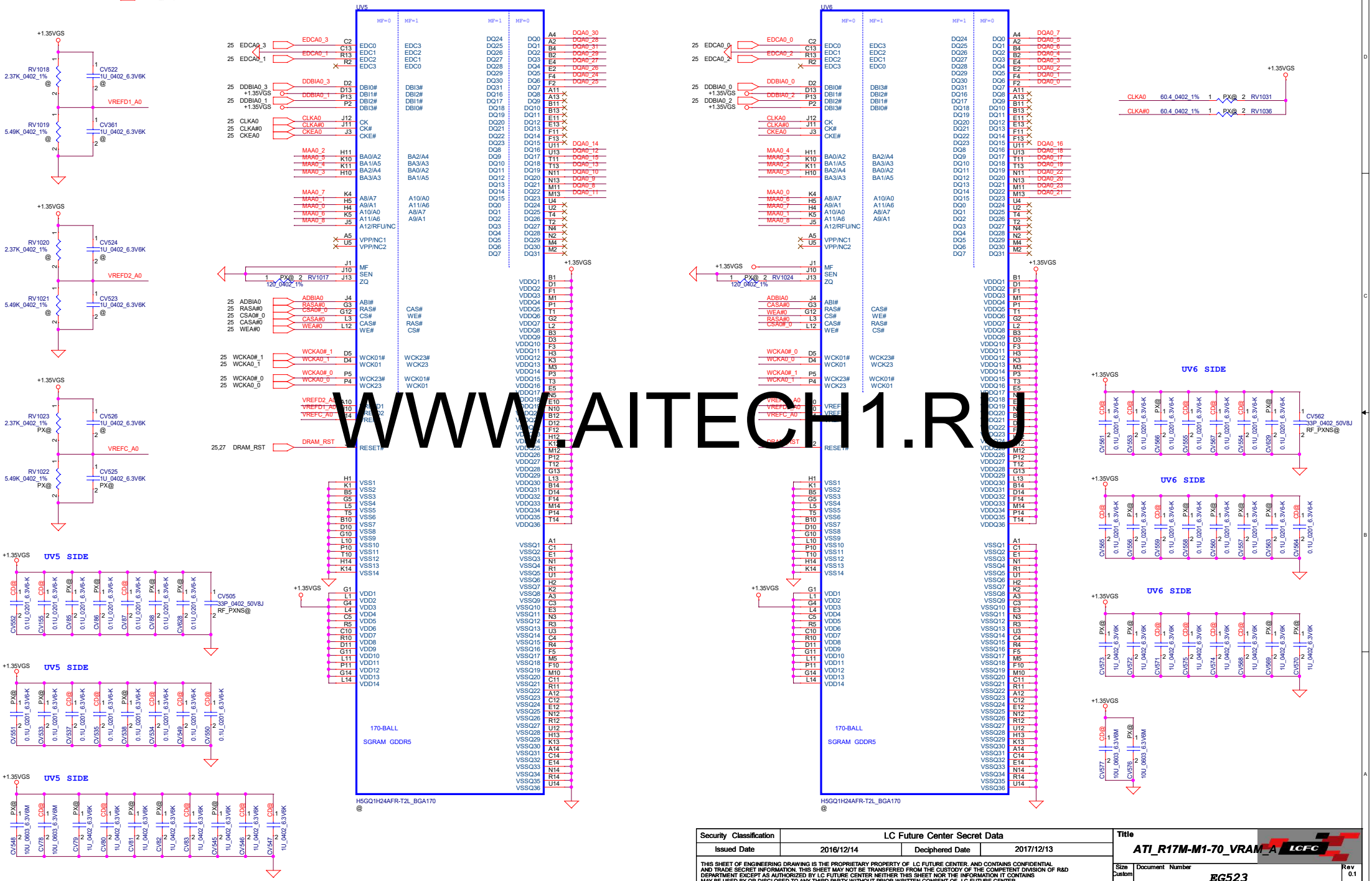
Lower 32 bits

DQA0_[31..0] 25

MAA0_[8..0] 25

MF=0 No Mirror

MF=1 Mirror



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Title: ATI_R17M-M1-70_VRAM_A

Size	Document Number	Rev
Custom	EG523	0.1

Date: Thursday, May 04, 2017 Sheet 26 of 60

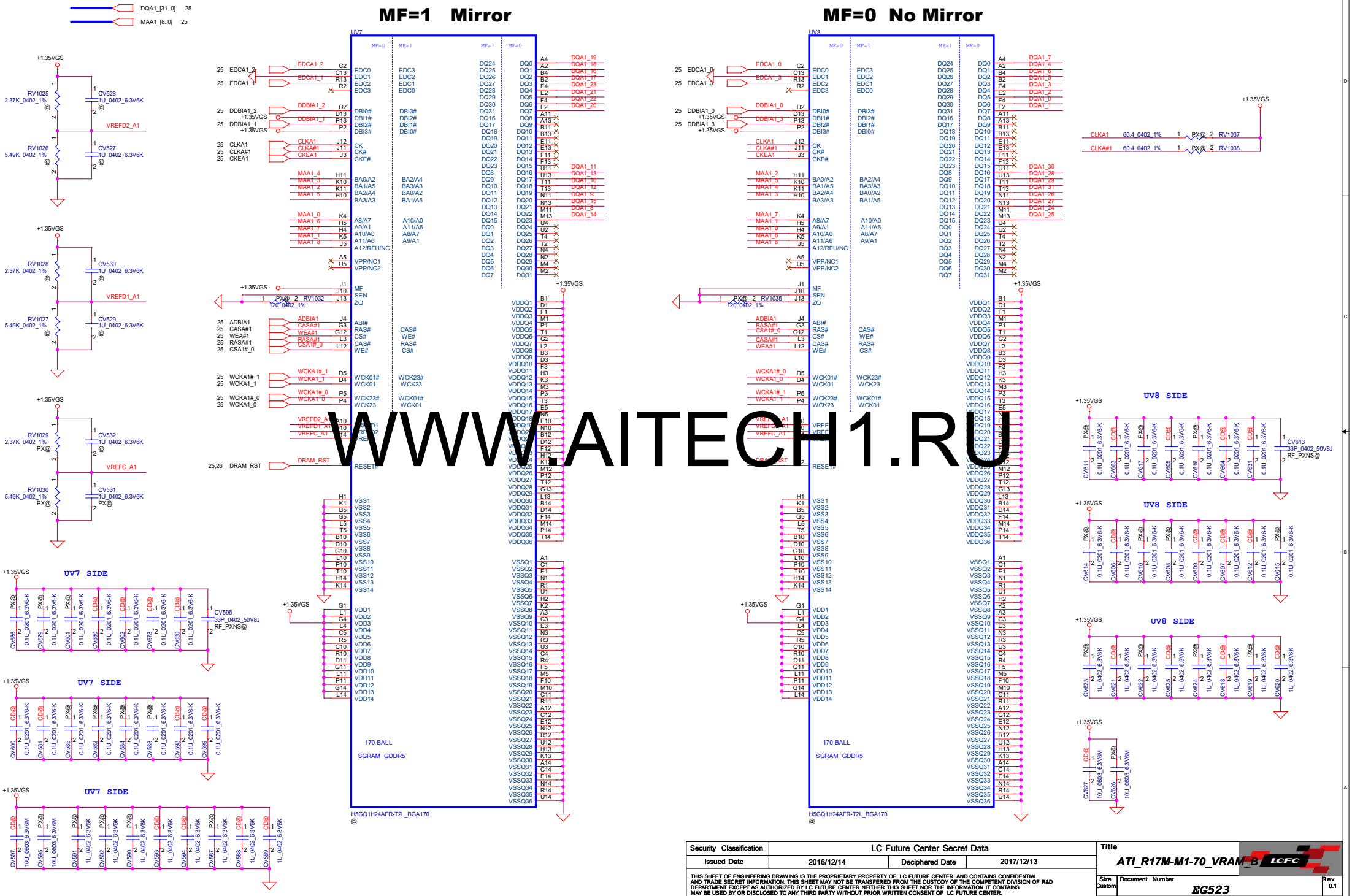
Upper 32 bits

DQA1_[31..0] 25

MAA1_[8..0] 25

MF=1 Mirror

MF=0 No Mirror



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Title: ATI_R17M-M1-70_VRAM_B

Size: Custom | Document Number: EG523 | Rev: 0.1

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Title: ***Blank***

Size	Document Number	Rev
Custom	***EG523***	0.1

Date: Thursday, May 04, 2017 Sheet 28 of 60

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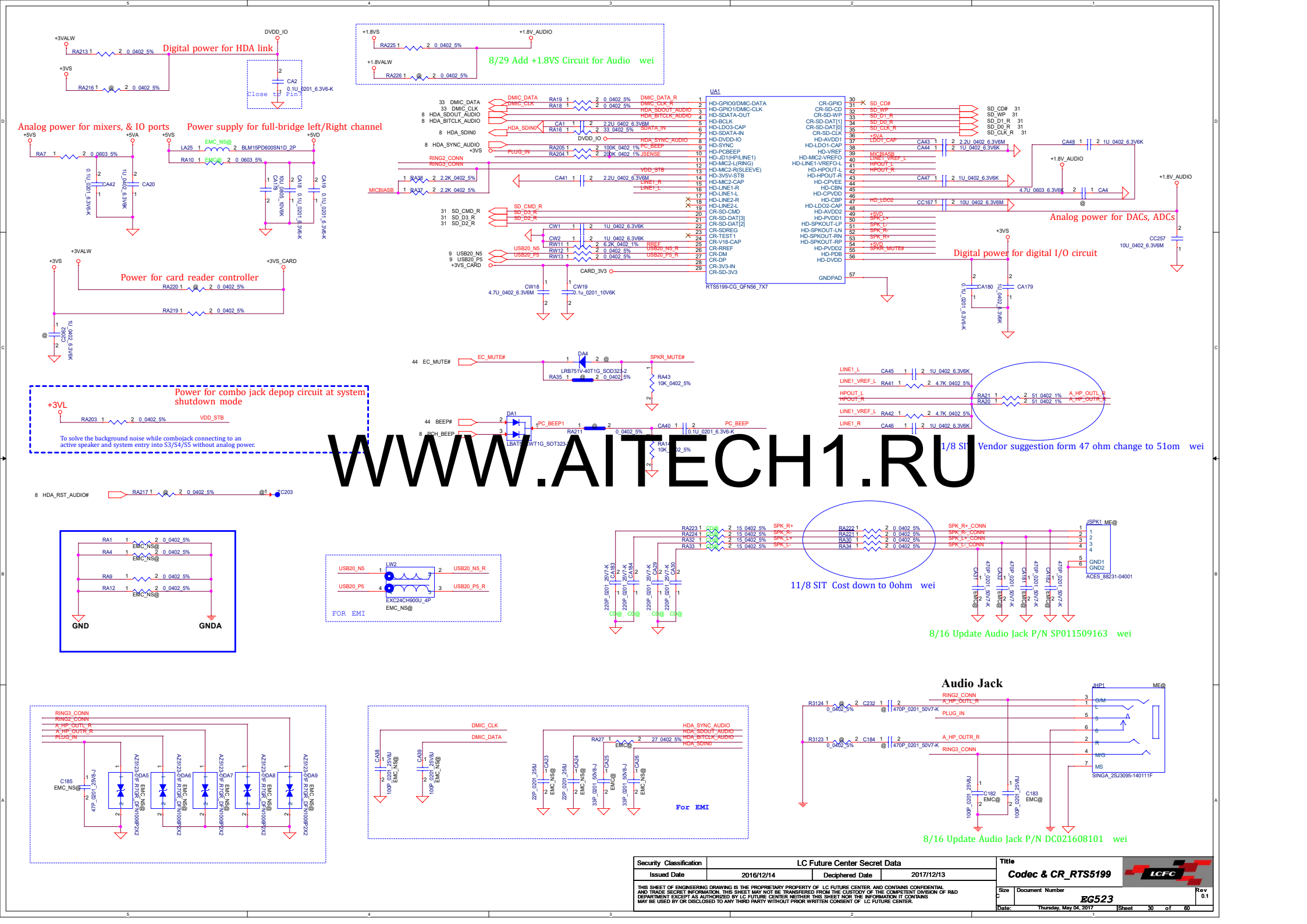
Title: ***Blank***

Size	Document Number	Rev
Custom	***EG523***	0.1

Date: Thursday, May 04, 2017 Sheet 29 of 60



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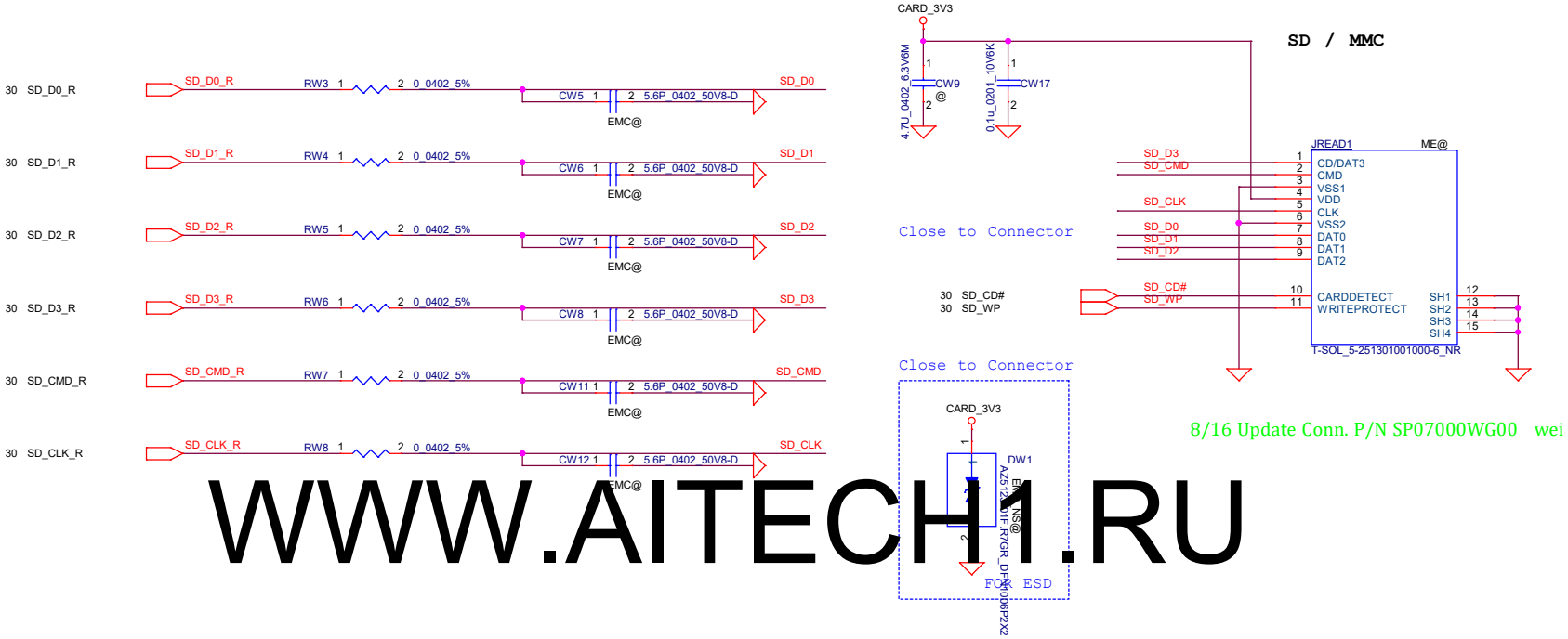
Title: Codec & CR_RTS5199

Size: C | Document Number: EG523 | Rev: 0.1

Date: Thursday, May 04, 2017 | Sheet 30 of 60



8/16 Update Conn. P/N SP07000WG00 wei

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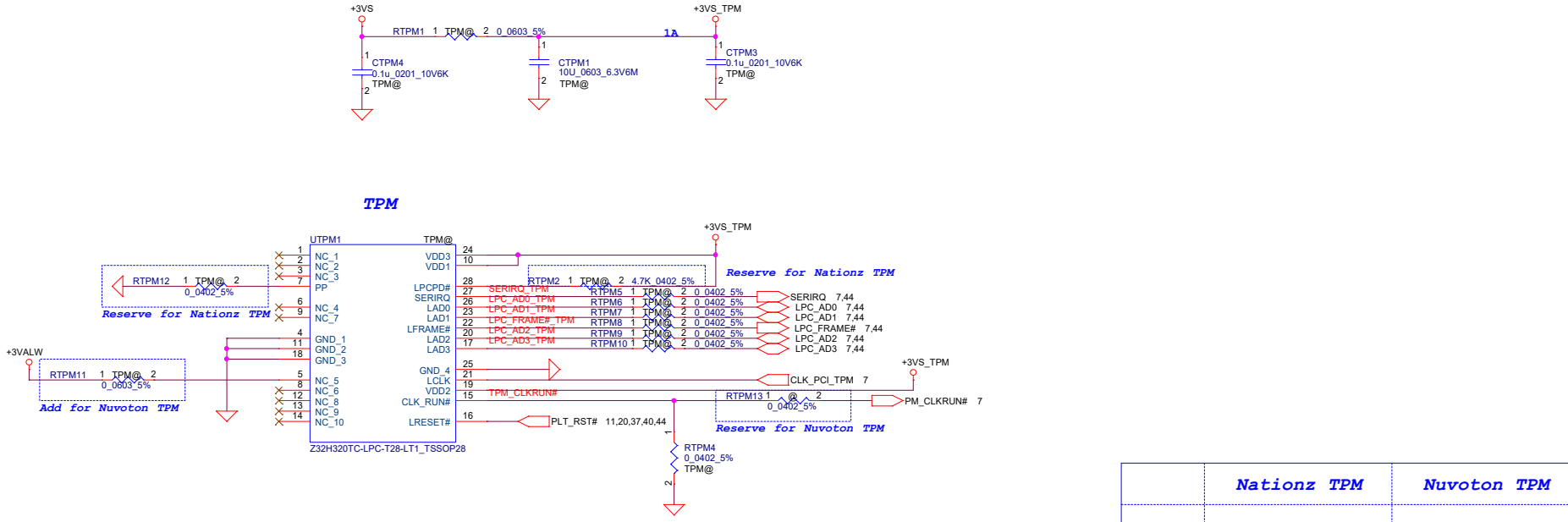
Title: **Cardreader**

Size	Document Number	Rev
Custom	EG523	0.1

Date: Thursday, May 04, 2017 Sheet 31 of 60



	Nationz TPM	Nuvoton TPM
RTPM2	Stuff	NC
RTPM12	Stuff	NC
RTPM11	NC	Stuff

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Title: TPM

Size	Document Number	Rev
Custom	EG523	0.1

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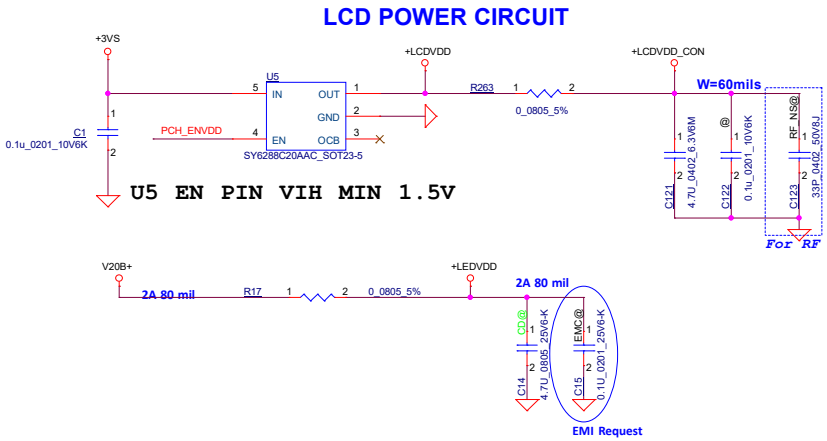

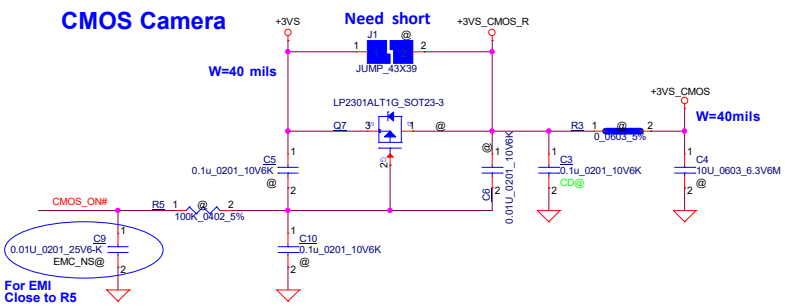

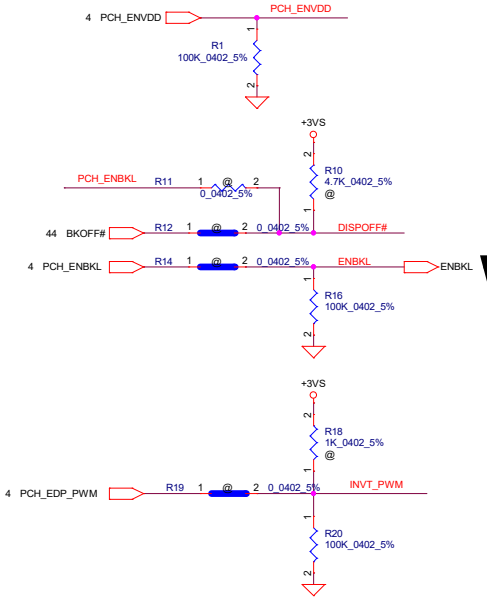

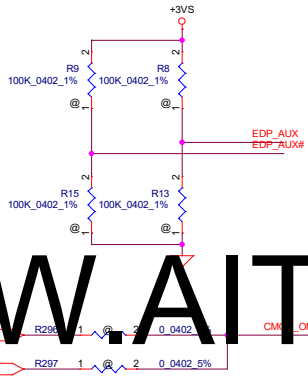

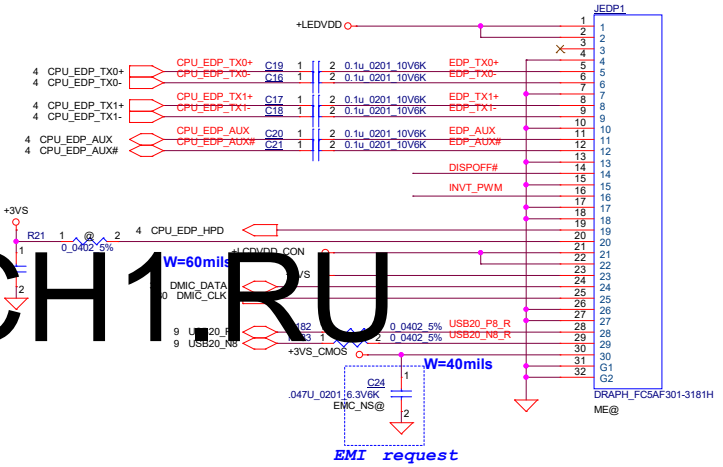

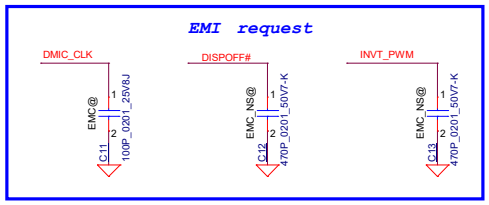

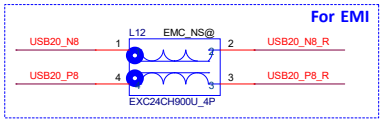

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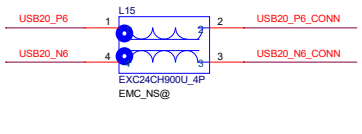
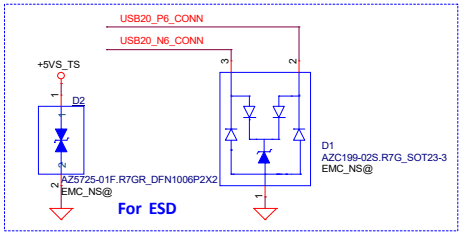
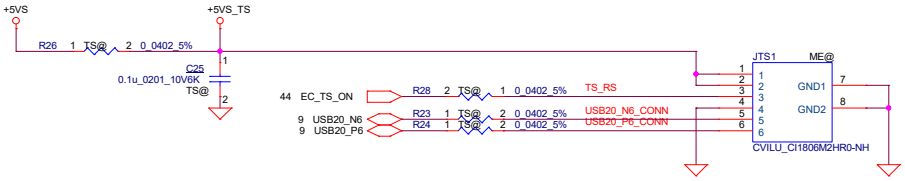
Touch Screen







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Title: eDP/CMOS/Touch screen

Size	Document Number	Rev
Custom	EG523	0.1

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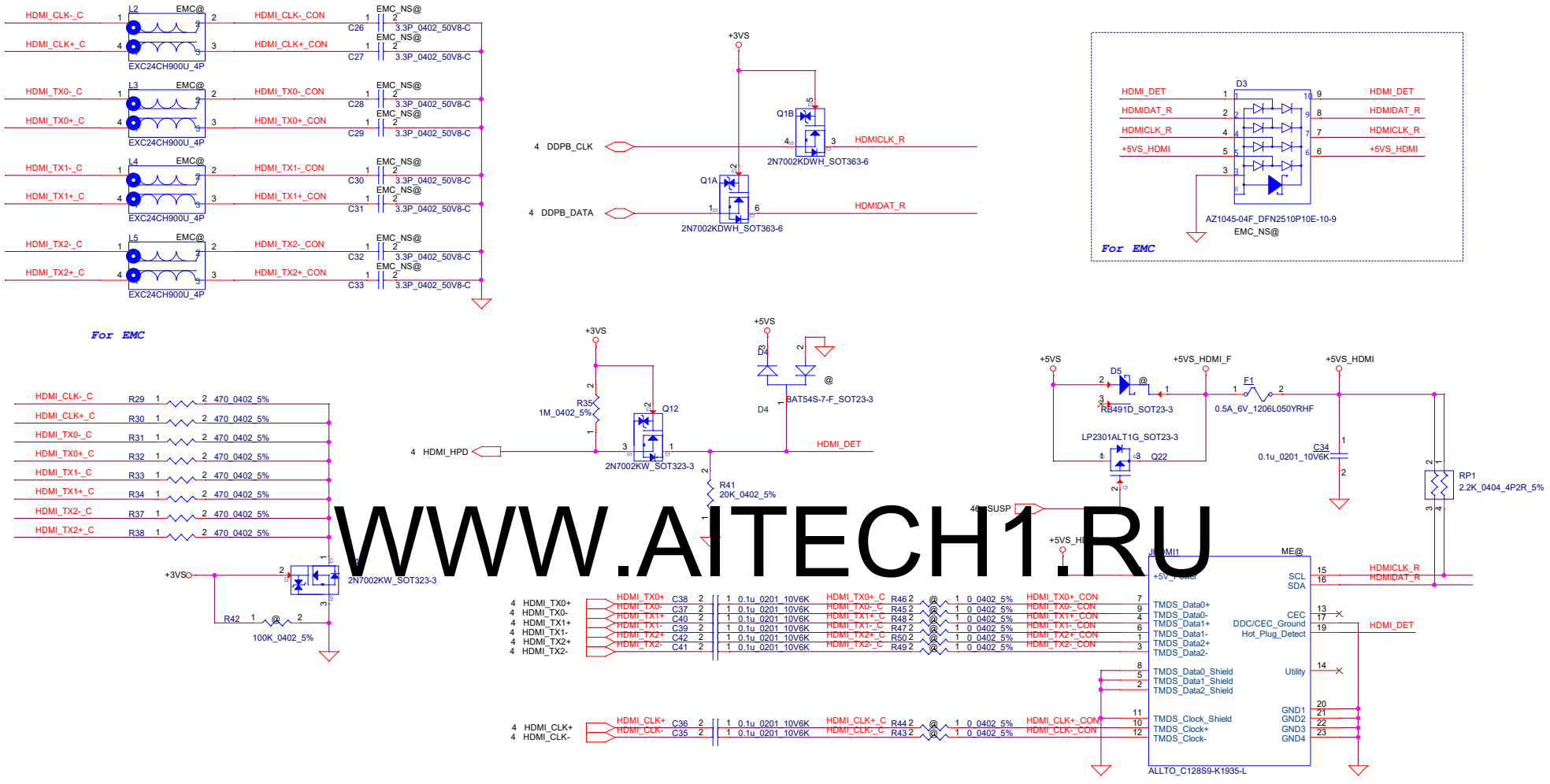

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8/16 Update HDMIConn. P/N DC021608081 wei

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Title: **HDMI_CONN**

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Custom	EG523	0.1

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Title: *P35-Blank*

Size	Document Number	Rev
Custom	*EG523*	0.1

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Title: ***Blank***

Size	Document Number	Rev
Custom	*EG523*	0.1

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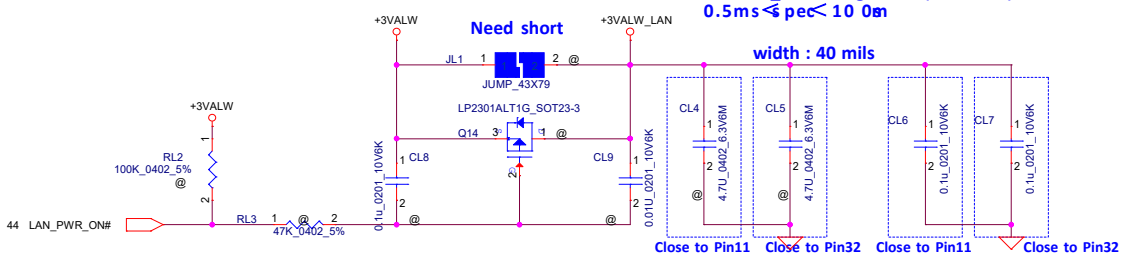
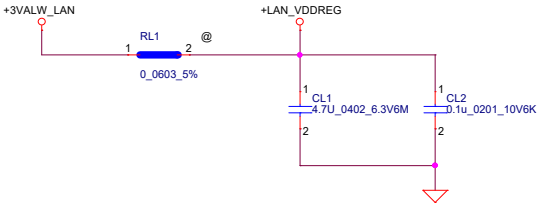
+3VALW TO +3VALW_LAN

+3VALW_LAN rising time (10%~90%)
0.5ms < spec < 10.0ms

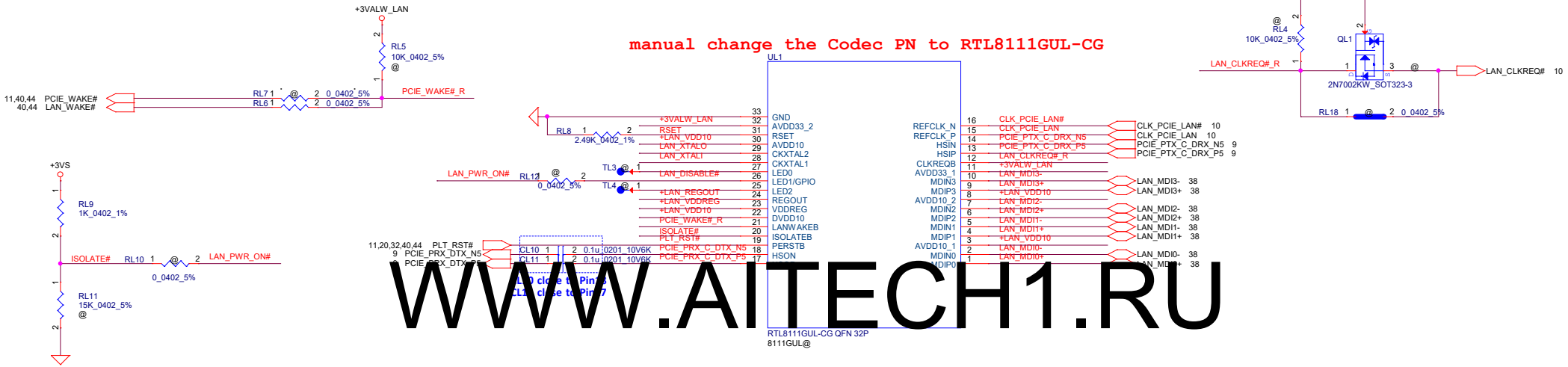
Need short

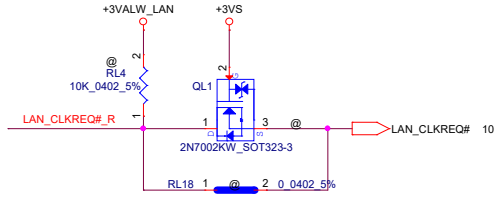
width : 40 mils

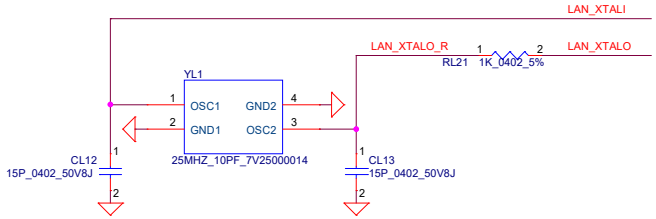


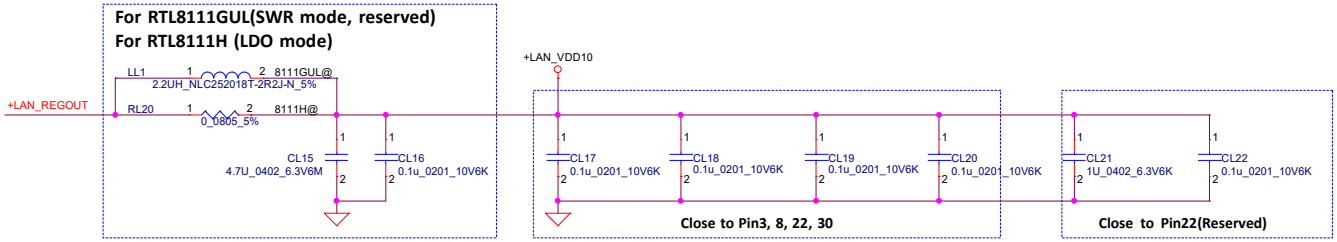


manual change the Codec PN to RTL8111GUL-CG









Layout Note: LL1 must be within 200mil to Pin24, CL15,CL16 must be within 200mil to LL1
+LAN_REGOUT: Width =60mil

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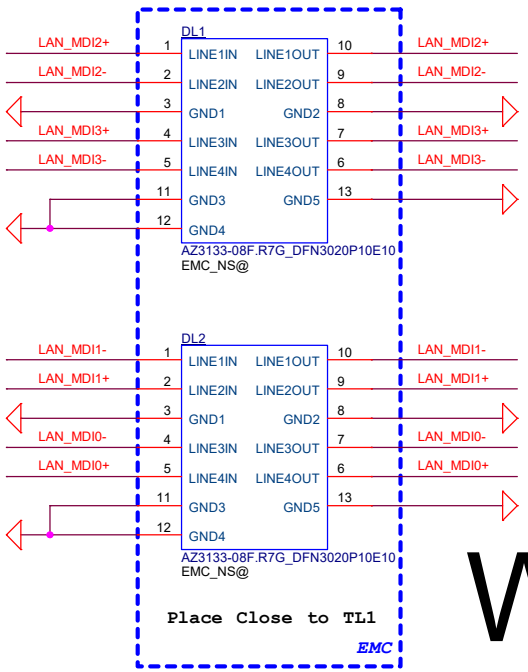
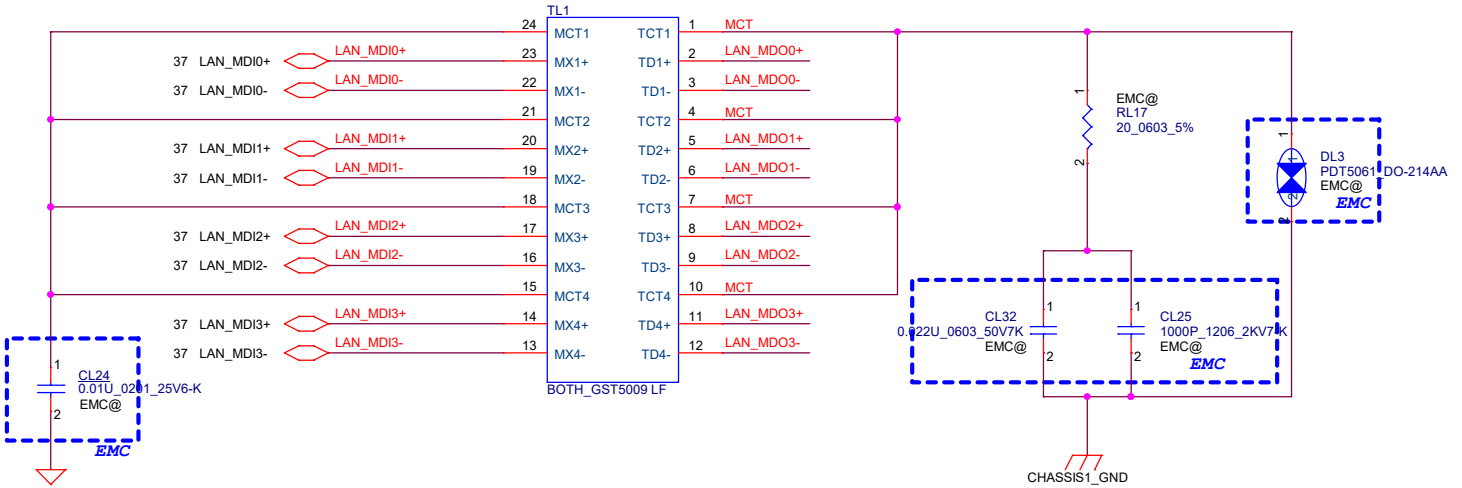
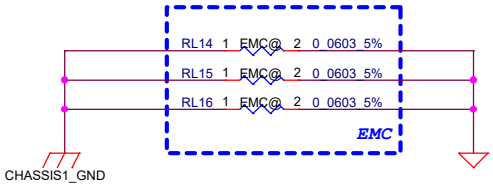
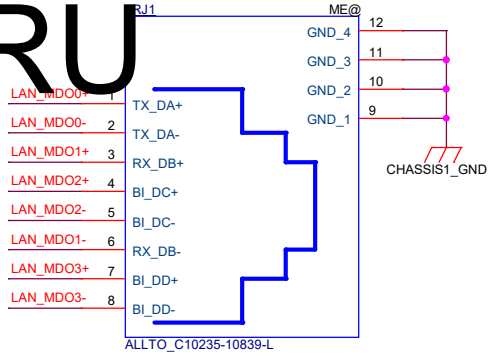
Title		
LAN_RTL8111H_CG		
Size: Custom	Document Number: EG523	Rev: 0.1
Date: Thursday, May 04, 2017	Sheet 37 of 60	

DL1/DL2
1'S PN:SC300003M00









8/16 Update RJ45 P/N DC021608091 wei

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Title: LAN_Transformer

Size	Document Number	Rev
B	EG523	0.1

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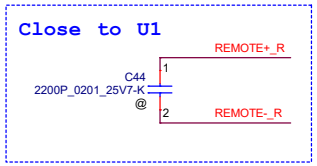

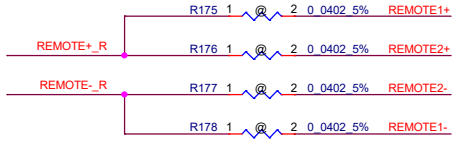

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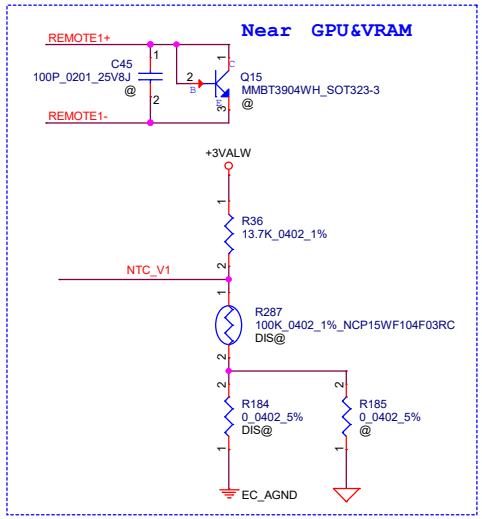
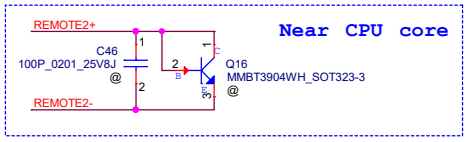
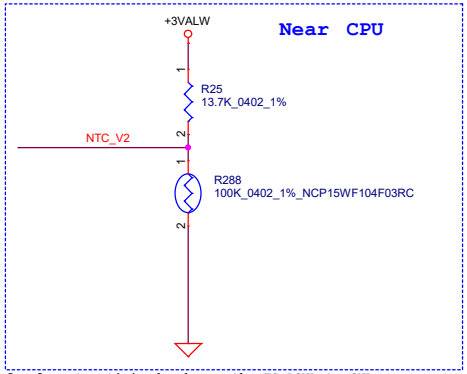
Trace length:<8"

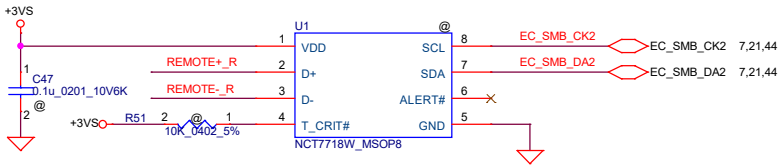






for layout optimized, change the EC_AGND to GND

SMSC thermal sensor placed near DIMM



Address 1001_101xb

HW thermal sensor

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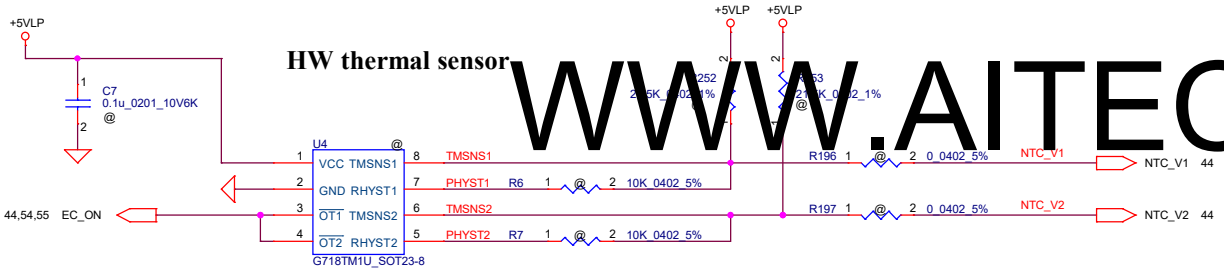
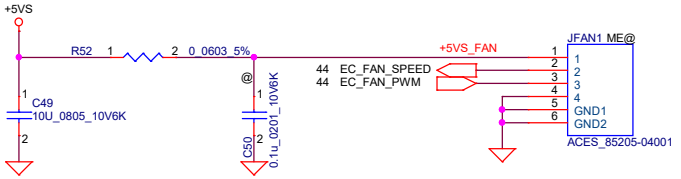


over temperature threshold:
RSET=3*RTMH
92+/-30C
Hysteresis temperature threshold.
RHYST=(RSET*RTML)/(3*RTML-RSET)
56+/-30C

FAN Conn



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Title: *Thermal sensor/FAN CONN*

Size	Document Number	Rev
Custom	EG523	0.1

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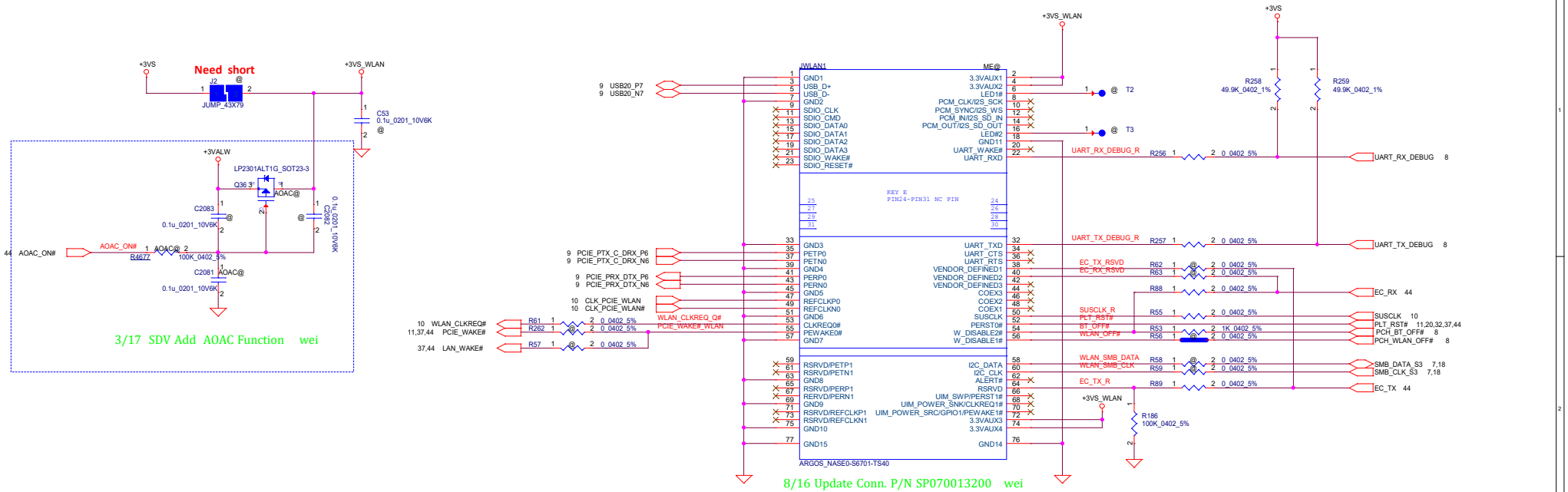
Mini-Express Card(WLAN/WiMAX)



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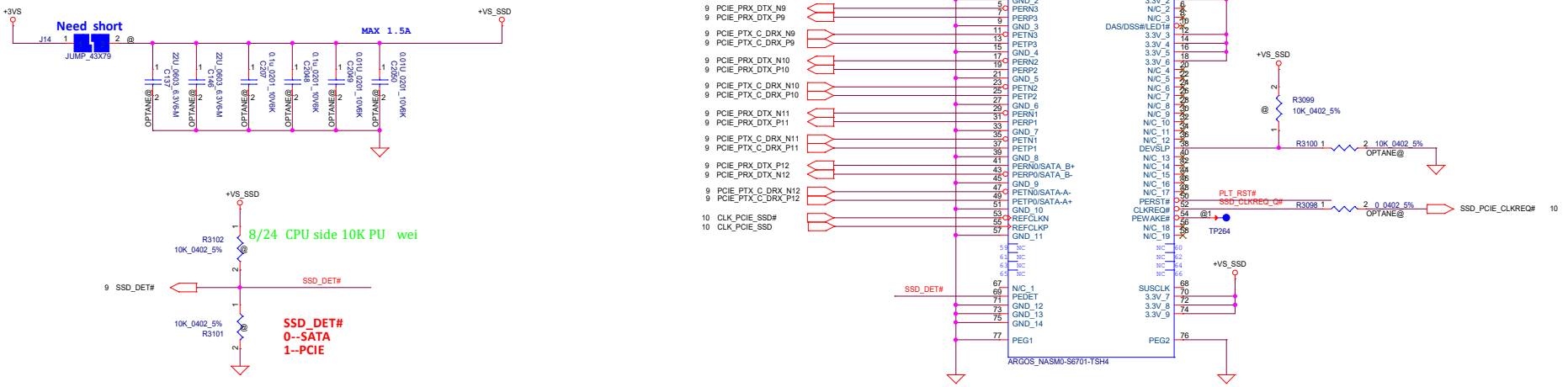
Optane Memory



Security Classification	LC Future Center Secret Data		
Issued Date	2016/12/14	Deciphered Date	2017/12/13

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Title: NGFF WLAN&SSD

Size	Document Number	Rev
C	EG523	0.1

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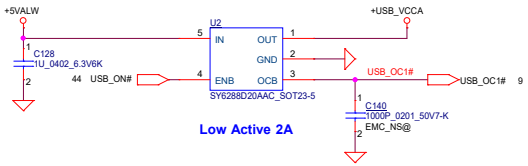
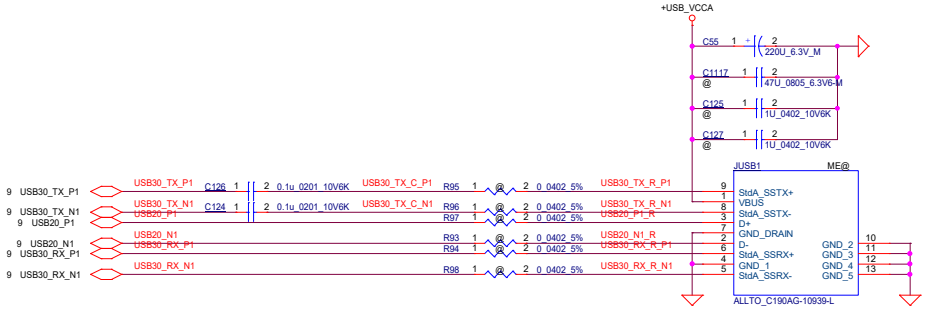
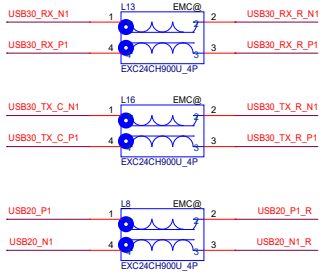
LEFT SIDE USB3.0 PORT x2



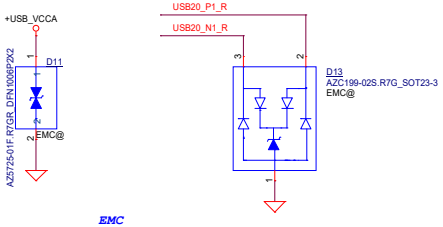
Low Active 2A



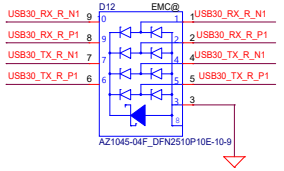
09/05 Update USBConn. P/N DC021609011 wei



EMC



EMC



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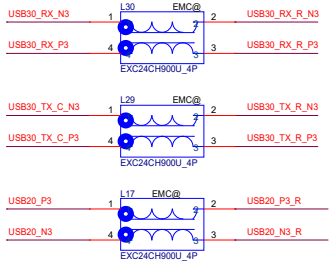
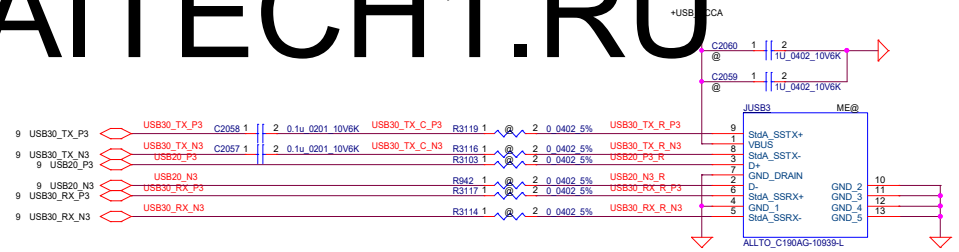
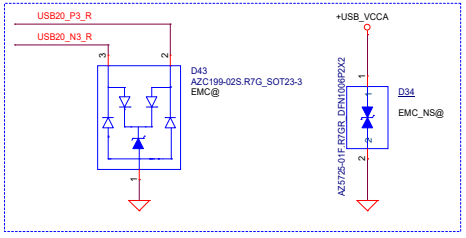
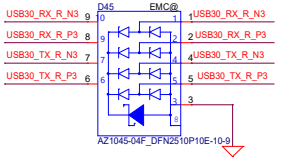




09/05 Update USBConn. P/N DC021609011 wei

FOR ESD Close to Connector





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Issued Date	2016/12/14	Deciphered Date	2017/12/13

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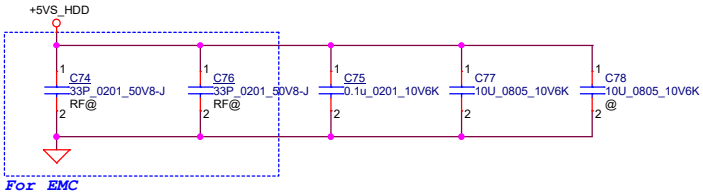
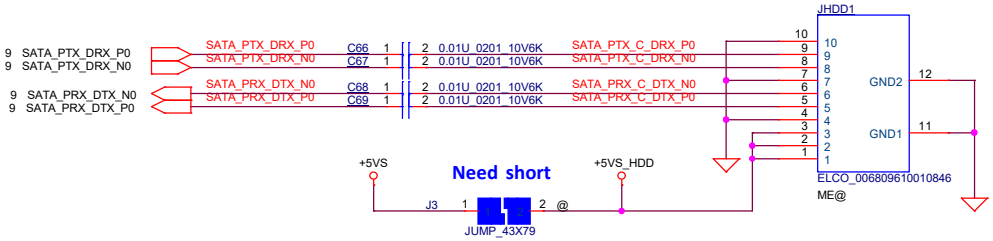
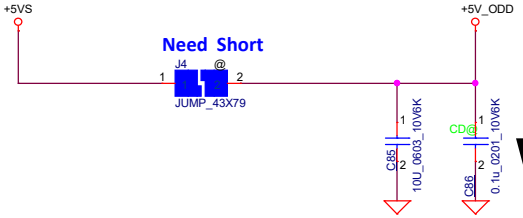
Title	USB3.0 PORT (LEFT)		
Size C	Document Number EG523		Rev 0.1
Date: Thursday, May 04, 2017	Sheet 41 of 60		

SATA HDD Conn.







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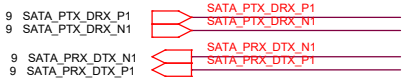
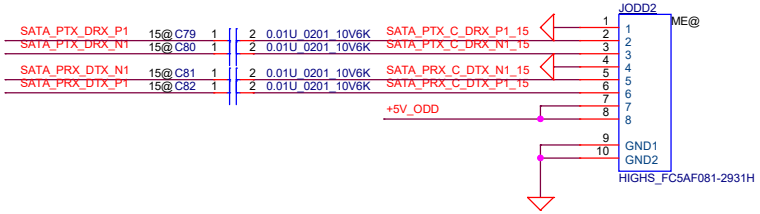
FOR 14"
SATA ODD Conn.



FOR 15" 17"
SATA ODD FFC Conn



8/16 Update Conn. P/N SP01001YV00 wei

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Issued Date	2016/12/14	Deciphered Date	2017/12/13

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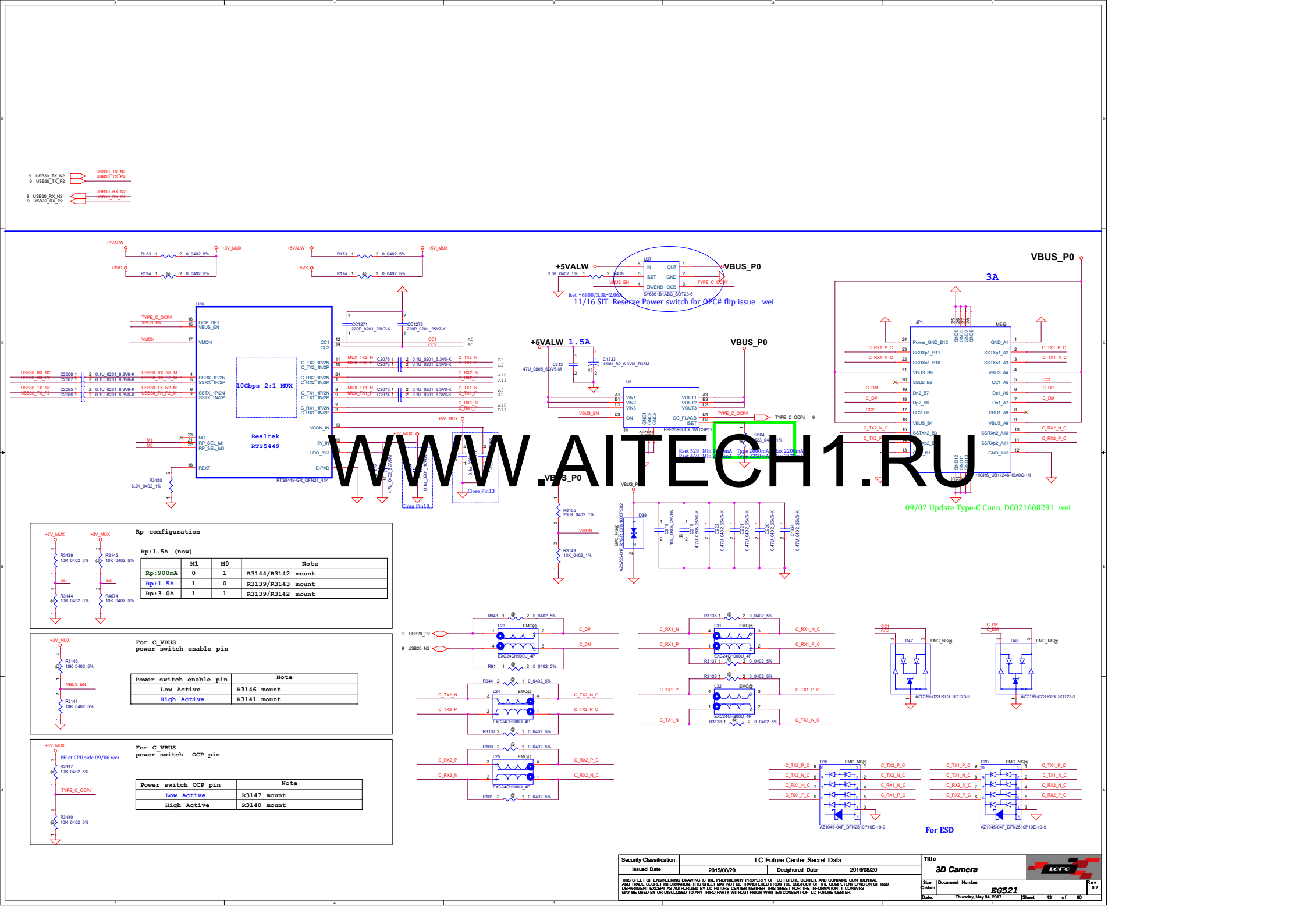
Title	HDD/ODD CONN		
Size: Custom	Document Number: EG523		Rev: 0.1
Date: Thursday, May 04, 2017	Sheet 42 of 60		



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Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

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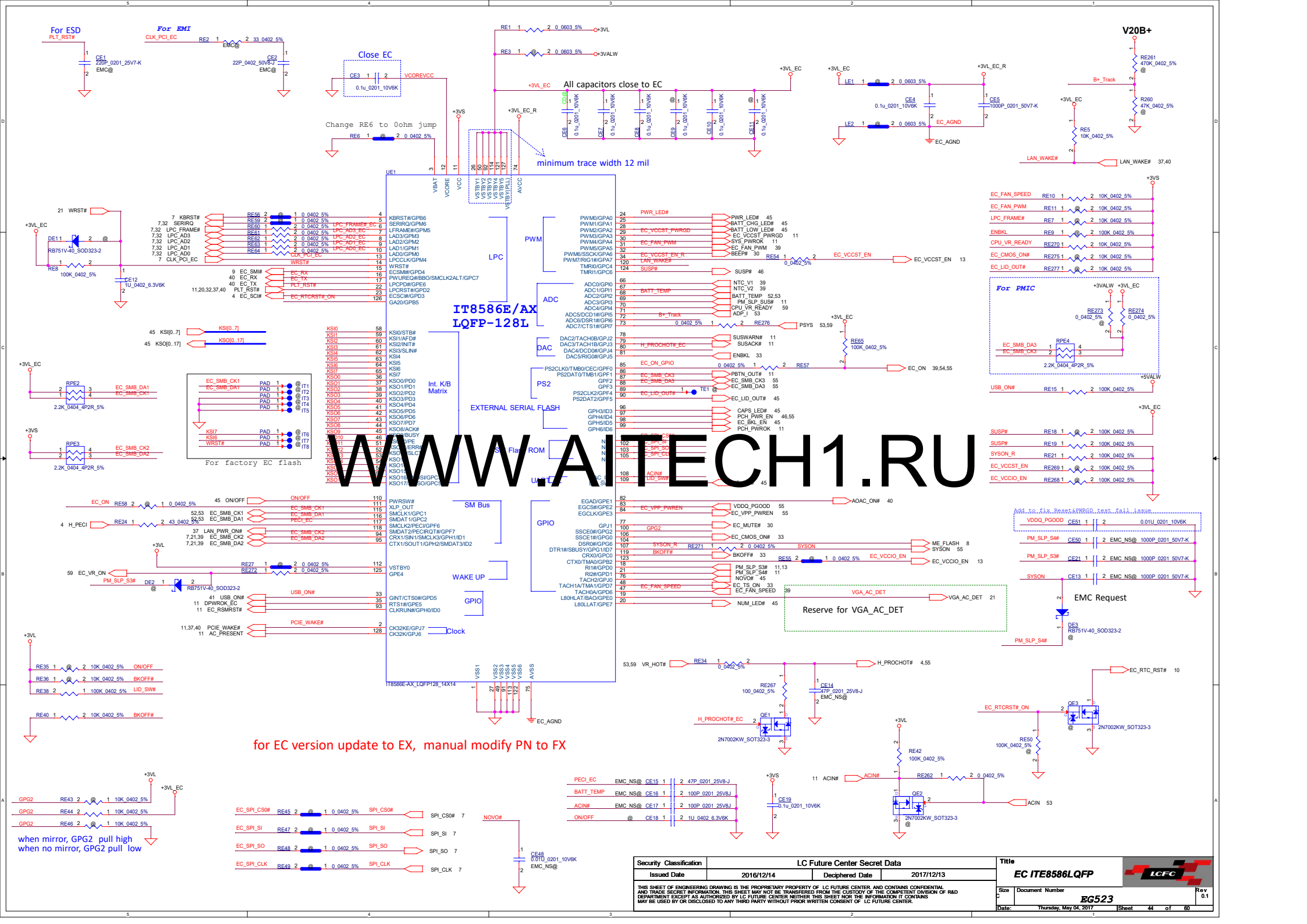
Title: 3D Camera

Size: Custom | Document Number: EG521 | Rev: 0.2

Date: Thursday, May 04, 2017 | Sheet 43 of 60



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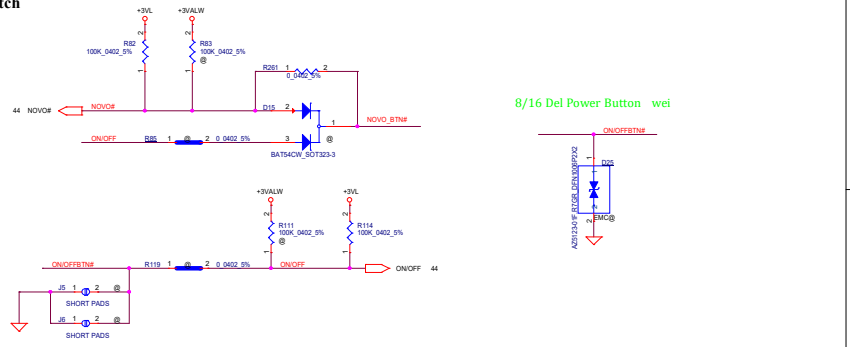
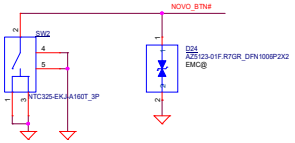
ON/OFF switch



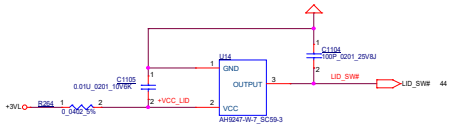
8/16 Del Power Button wei

Novo button

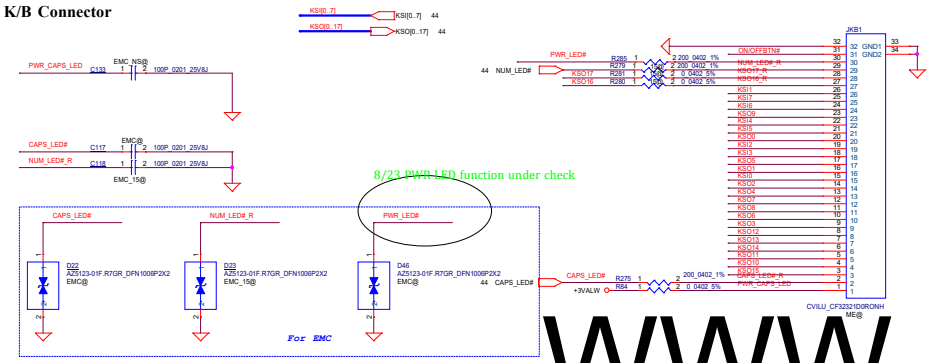


8/31 Update the P/N SN100008W00 wei

LID switch

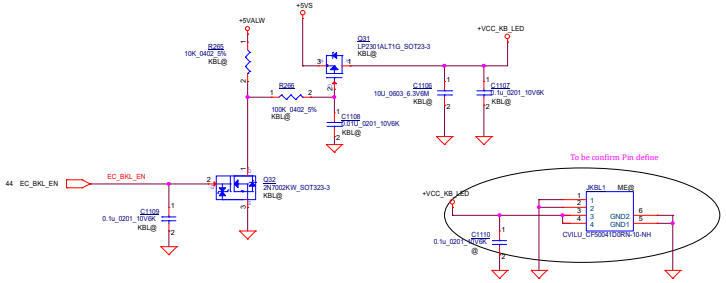


K/B Connector



8/23 PWR LED function under check

KB Backlight Connector



8/31 Update K[illegible] Conn. P/N SP[illegible]160824[illegible] wei

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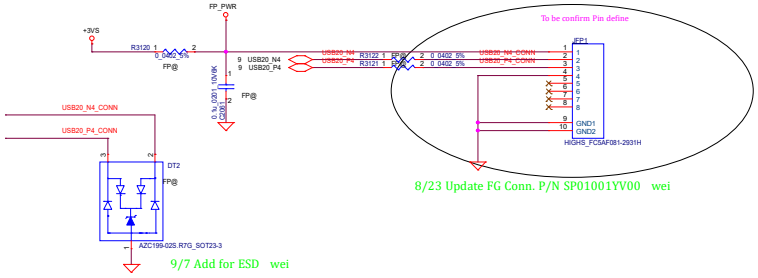
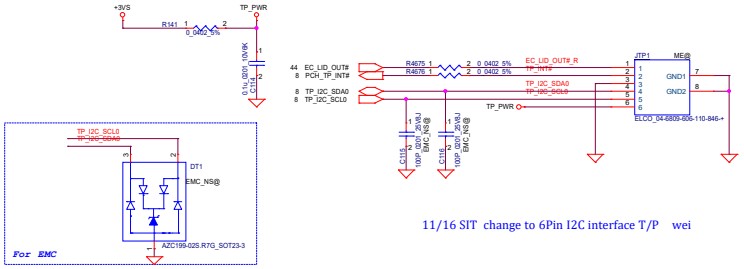
Finger Print Connector



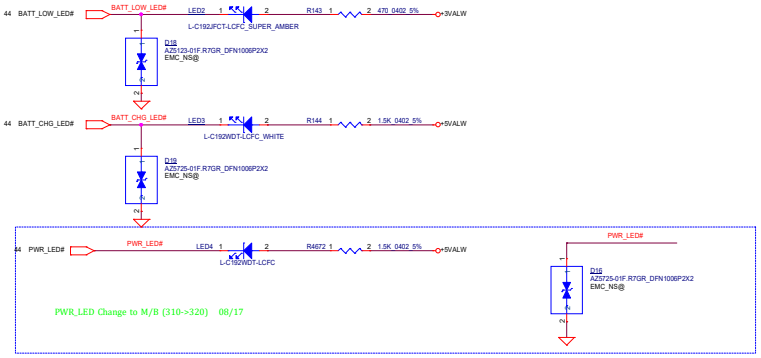
8/23 Update FG Conn. P/N SP01001YV00 wei

9/7 Add for ESD wei

TP/B Connector



11/16 SIT change to 6Pin I2C interface T/P wei



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Issued Date	2016/12/14	Deciphered Date	2017/12/13

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Title: KBD/PWR/IO/LED/TP Conn.

Size	Document Number	Rev
Custom	EG523	0.1

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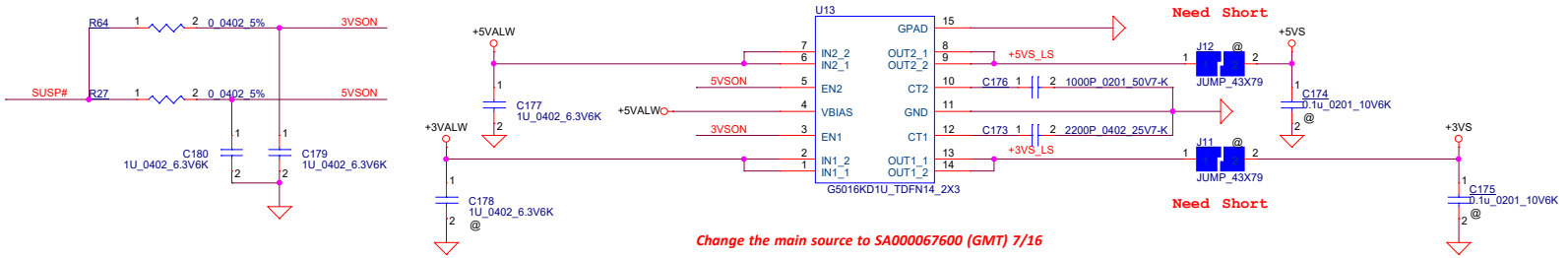
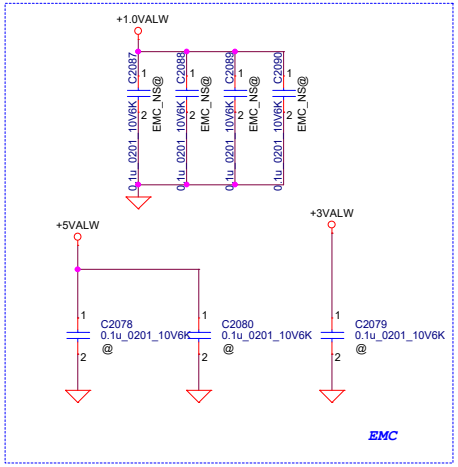
Load Switch
+5VALW To +5VS
+3VALW To +3VS

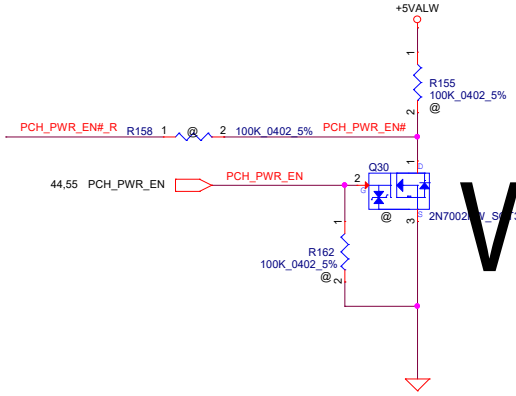
+3VS, C173 --> 2.74ms
+5VS, C176 --> 2.03ms

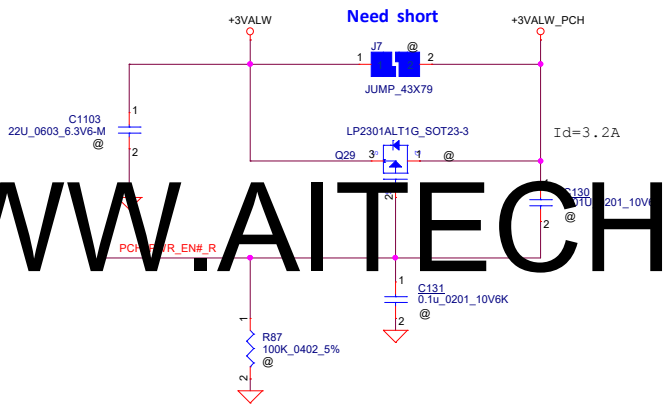
VIN 5V and 3.3V (VBIAS=5V), IMAX(per channel)=6A, Rds=16mohm

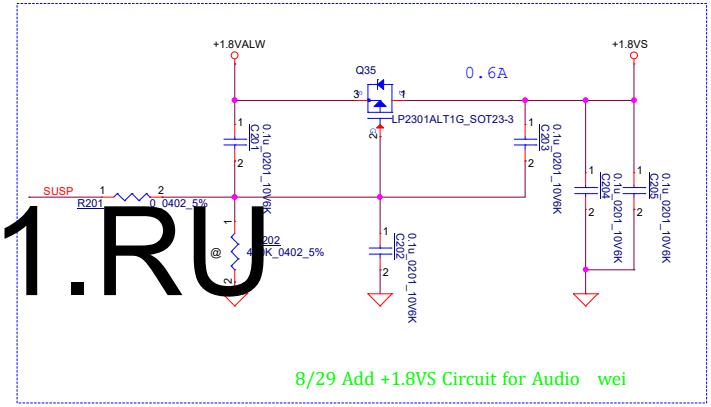


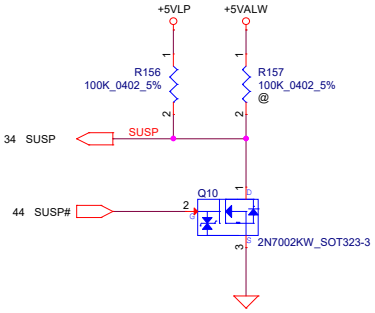
Change the main source to SA000067600 (GMT) 7/16



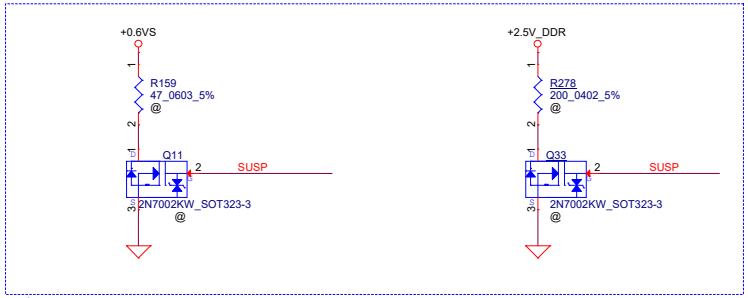








For DisCharge



08/29: Need double check enable signal and the resistance

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Title: **DC V TO VS INTERFACE**

Size	Document Number	Rev
Custom	EG523	0.1

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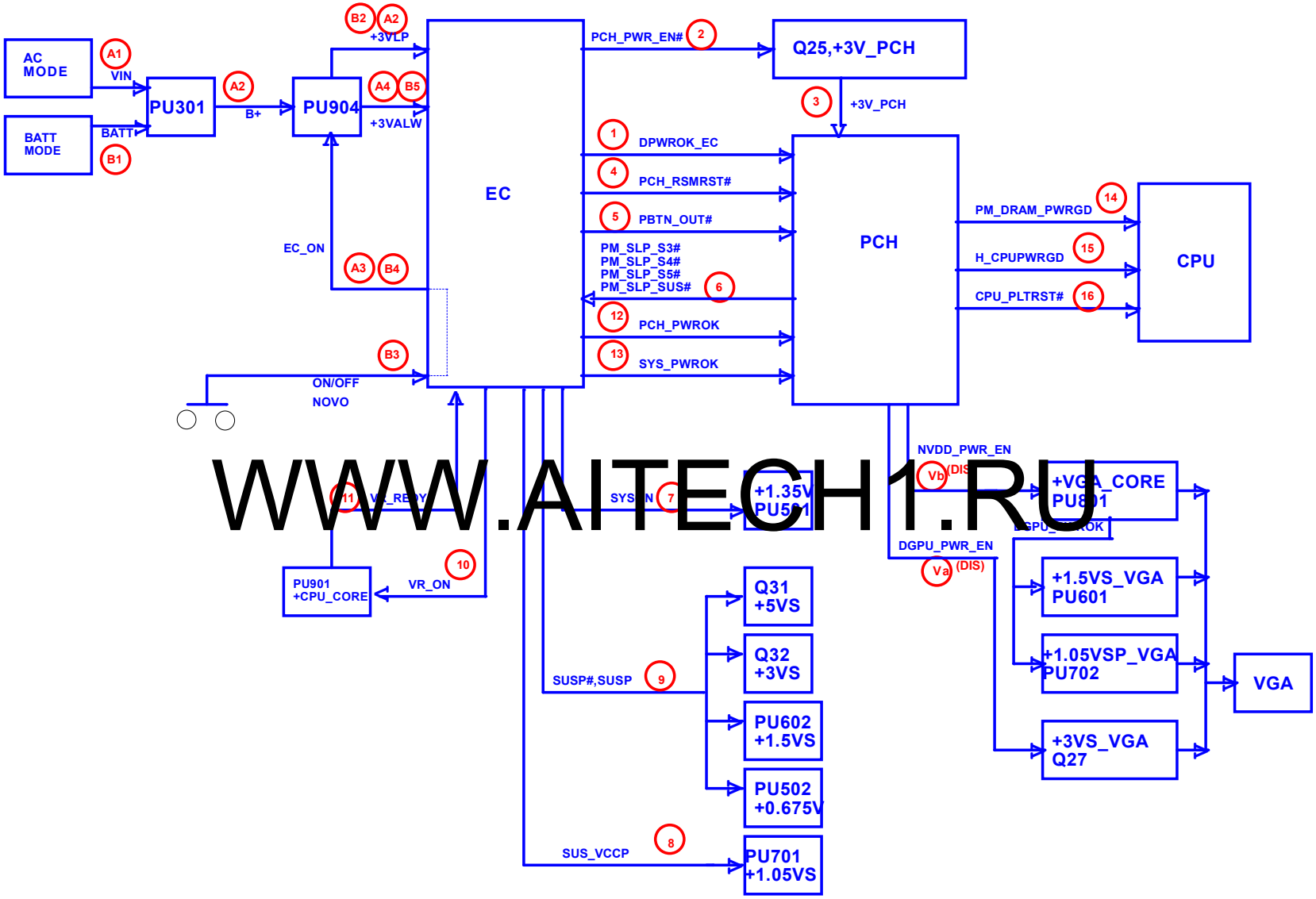

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Title: **Power sequence block**

Size	Document Number	Rev
Custom	EG523	0.1

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ZZZ1 NMB453@

NM-B453
DA60001 3Q00
I+A

PCB_MB

UC1 I7@

KBL-R CPU
SA00008J600

UC1 I5@

KBL-R CPU
SA00008J500

CPU

CPU

UL1 8111H@

RTL8111H-CG
SA000074W00

LAN Chip

UV1 PX@

R17M-M1-70 GPU
SA000086K00

GPU

ZZZ2 DRAM_S4G@

Samsung
X7643712009

ZZZ2 DRAM_M4G@

Micron
X7643712008

ZZZ2 DRAM_H4G@

Hynix
X7643712007

2400MT/s DRAM X76 BOM

ZZZ4 S4GX4@

Samsung
X7643912002

ZZZ4 H4GX4@

Hynix
X7643912001

ZZZ4 M4GX4@

Micron
X7643912003

ZZZ4 S8GX4@

Samsung
X7643A12002

ZZZ4 H8GX4@

Hynix
X7643A12001

ZZZ4 M8GX4@

Micron
X7643A12003

VRAM X76 BOM

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ZZZ3 HDMI@

HDMI PN
RO00000040J

HDMI Royalty

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Title: *Virtual symbol*

Size	Document Number	Rev
C	DG42A	0.2

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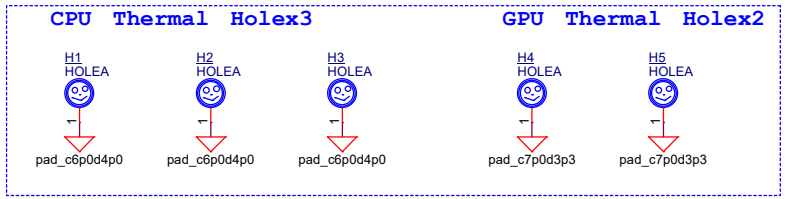

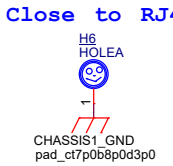

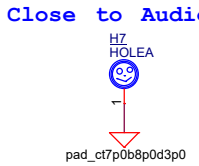

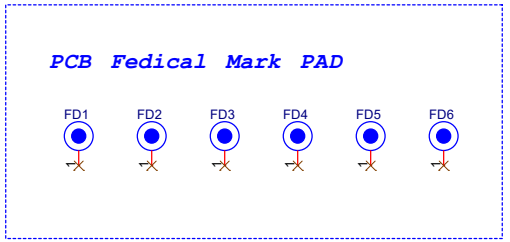

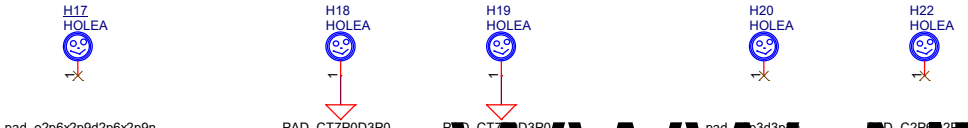

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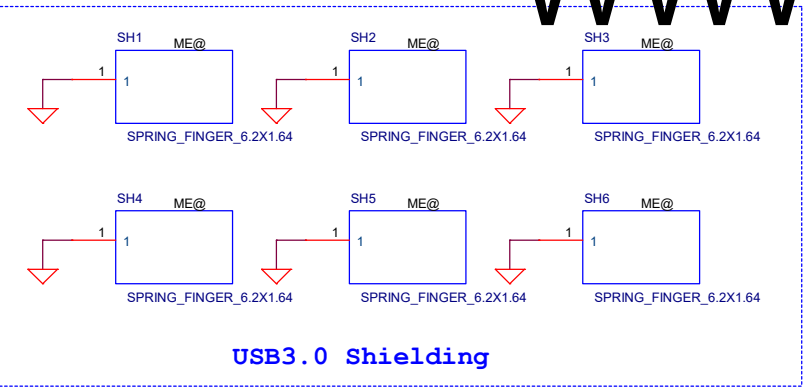

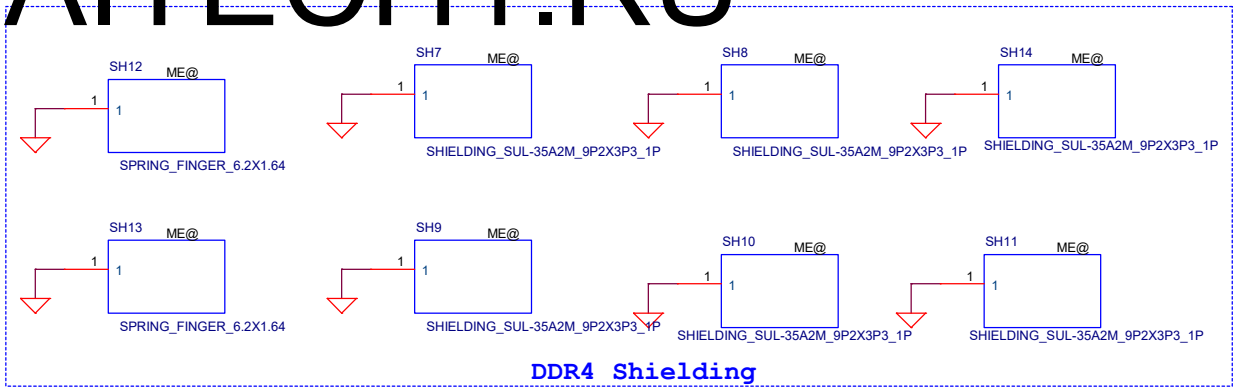

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Title	Hole		
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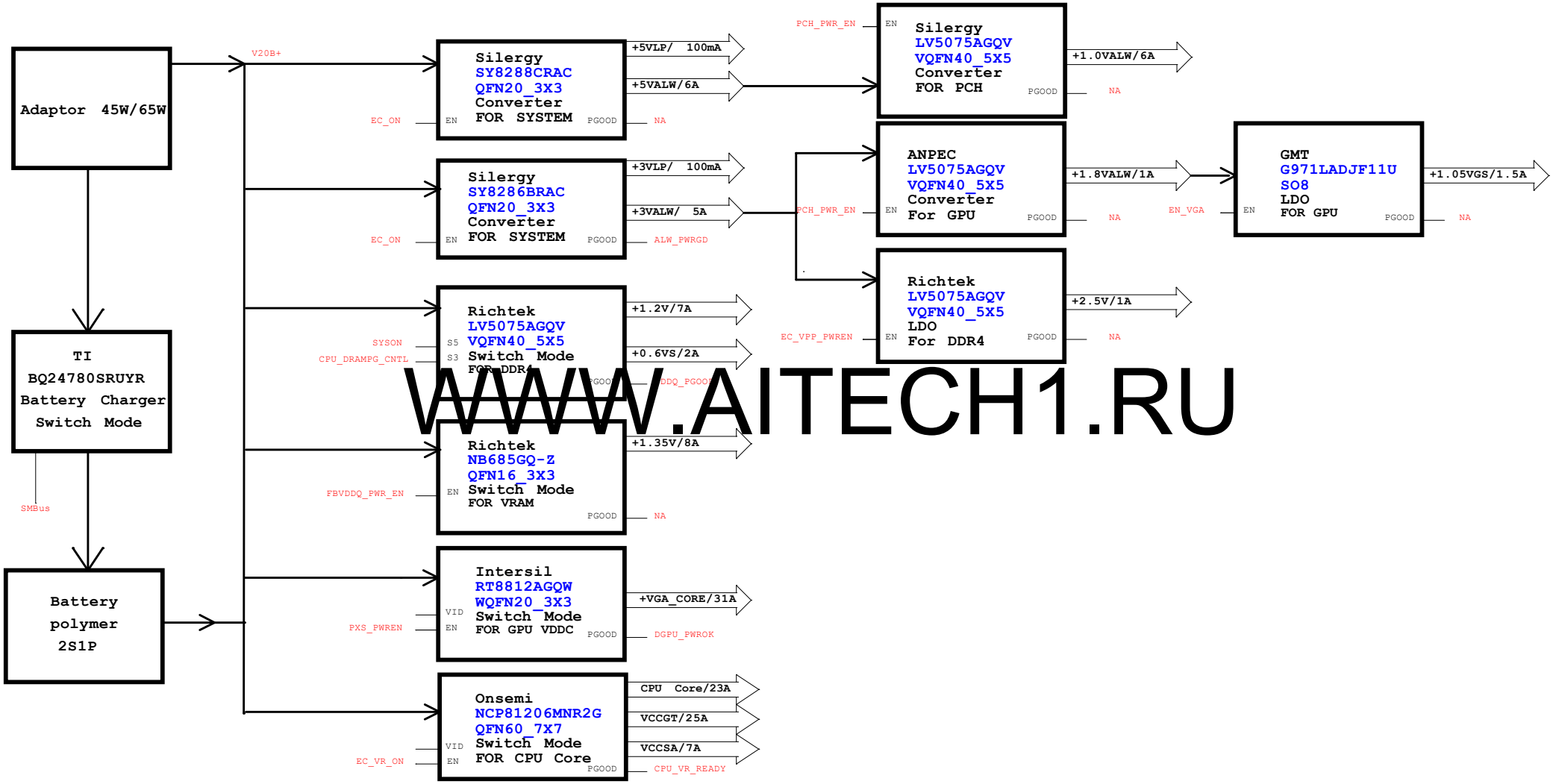
B	EG523		0.1
Date:	Thursday, May 04, 2017	Sheet	49 of 60



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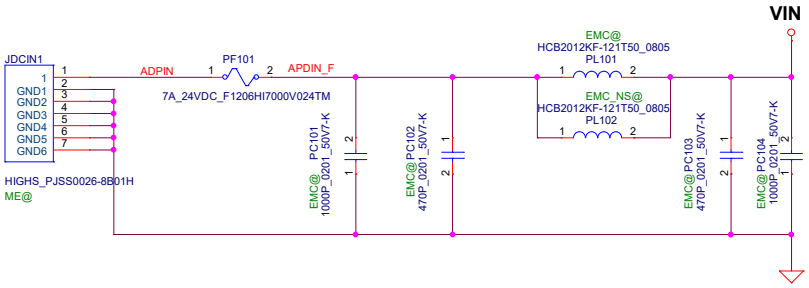
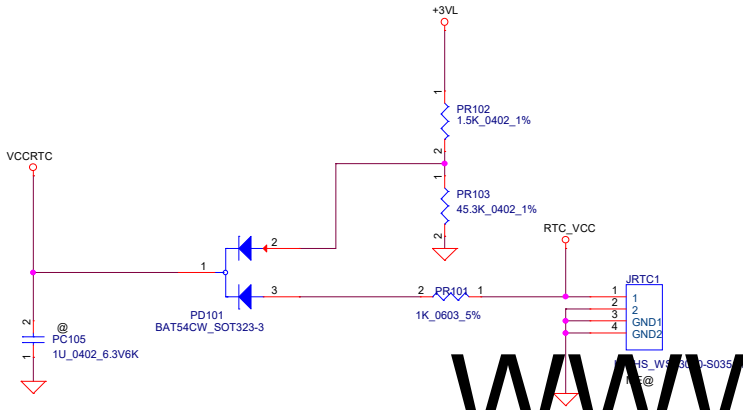
Title: PWR-Power Diagram

Size	Document Number	Rev
Custom	DG42A	0.1

Date: Thursday, May 04, 2017 Sheet 50 of 60





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RTC_VCC 20MIL
+3VL 20MIL
VCCRTC 20MIL

No charge RTC with 35mm cable

RTC Battery for GCM BOM
(2nd source and quoted price)

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Title: PWR-DCIN / RTC charger

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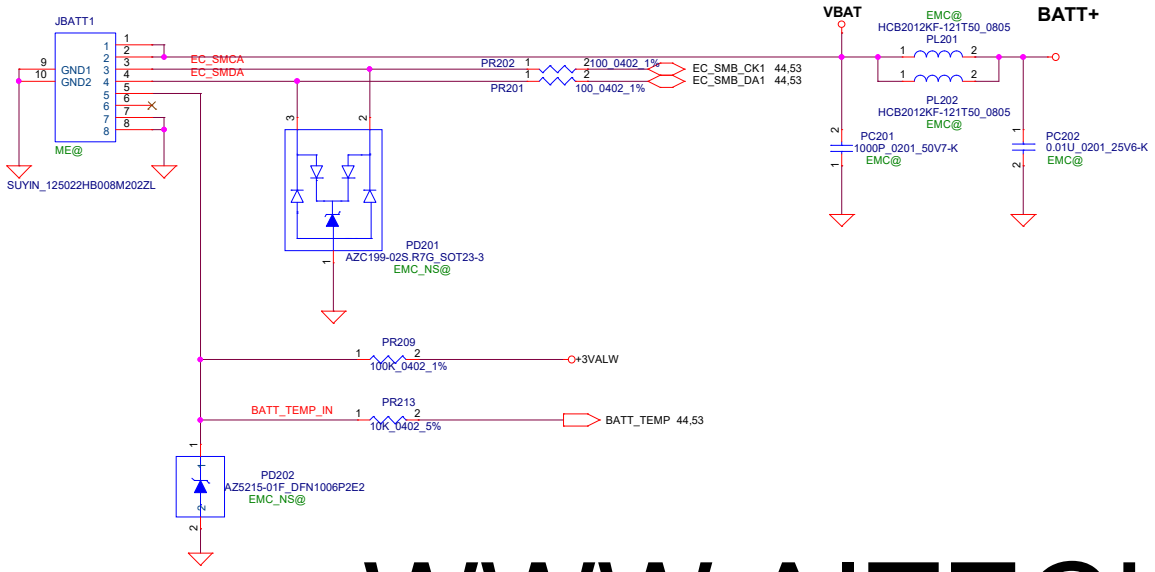

2S1P polymer battery voltage level: +6V ~ 8.4 V

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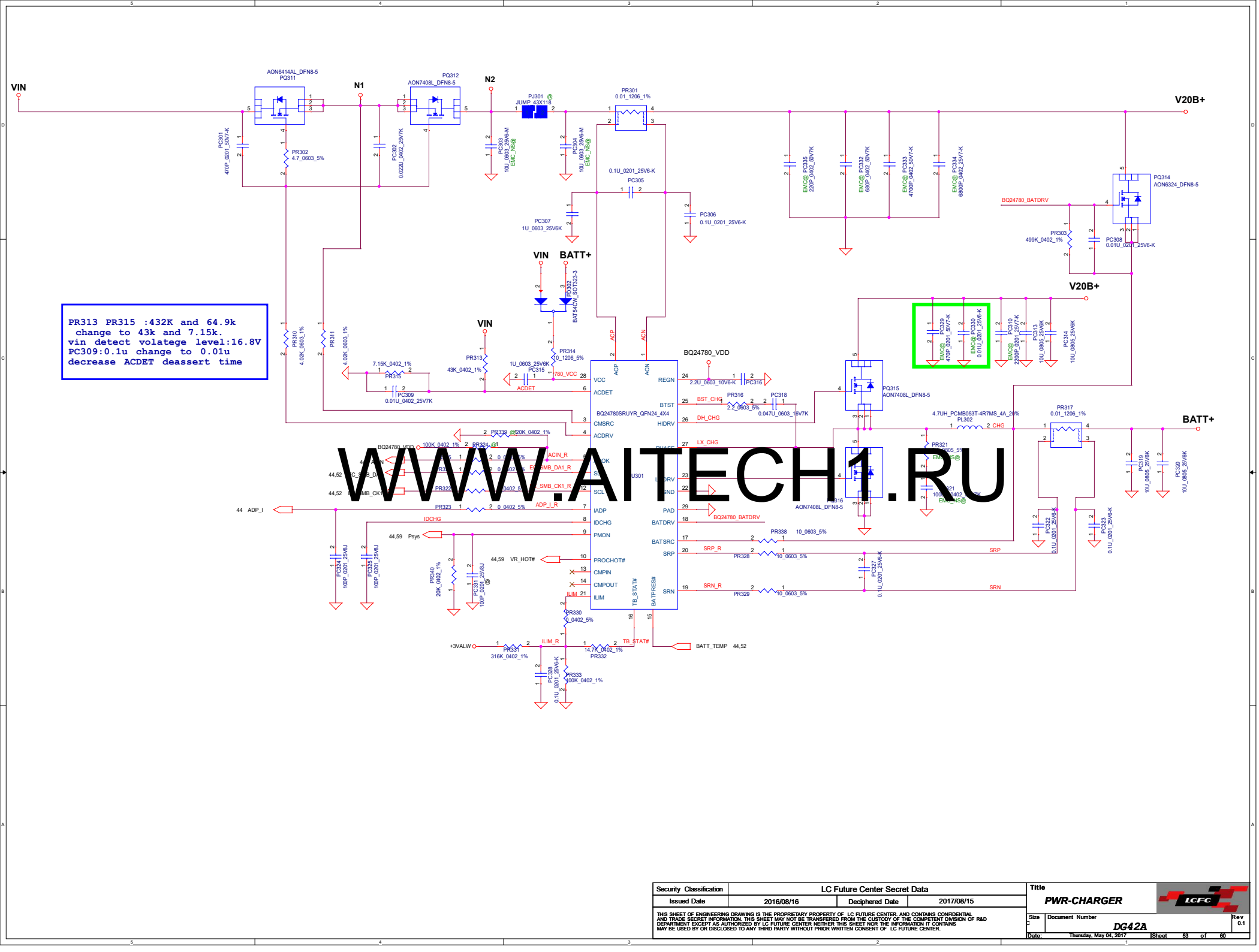
Title: PWR-BATTERY CONN/OTP

Size	Document Number	Rev
Custom	DG42A	0.1

Date: Thursday, May 04, 2017 Sheet 52 of 60


PR313 PR315 :432K and 64.9k
change to 43k and 7.15k.
vin detect volatege level:16.8V
PC309:0.1u change to 0.01u
decrease ACDET deassert time
VIN
N1
N2
V20B+
BATT+
BQ24780SRUYR_QFN24_4X4
BQ24780_VDD
BQ24780_BATDRV
AON6414AL_DFN8-5
AON7408L_DFN8-5
AON6324_DFN8-5
BAT54CW_SOT323-3
4.7UH_PCMB053T-4R7MS_4A_20%
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Issued Date
2016/08/16
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Title
PWR-CHARGER
Size
C
Document Number
DG42A
Rev
0.1
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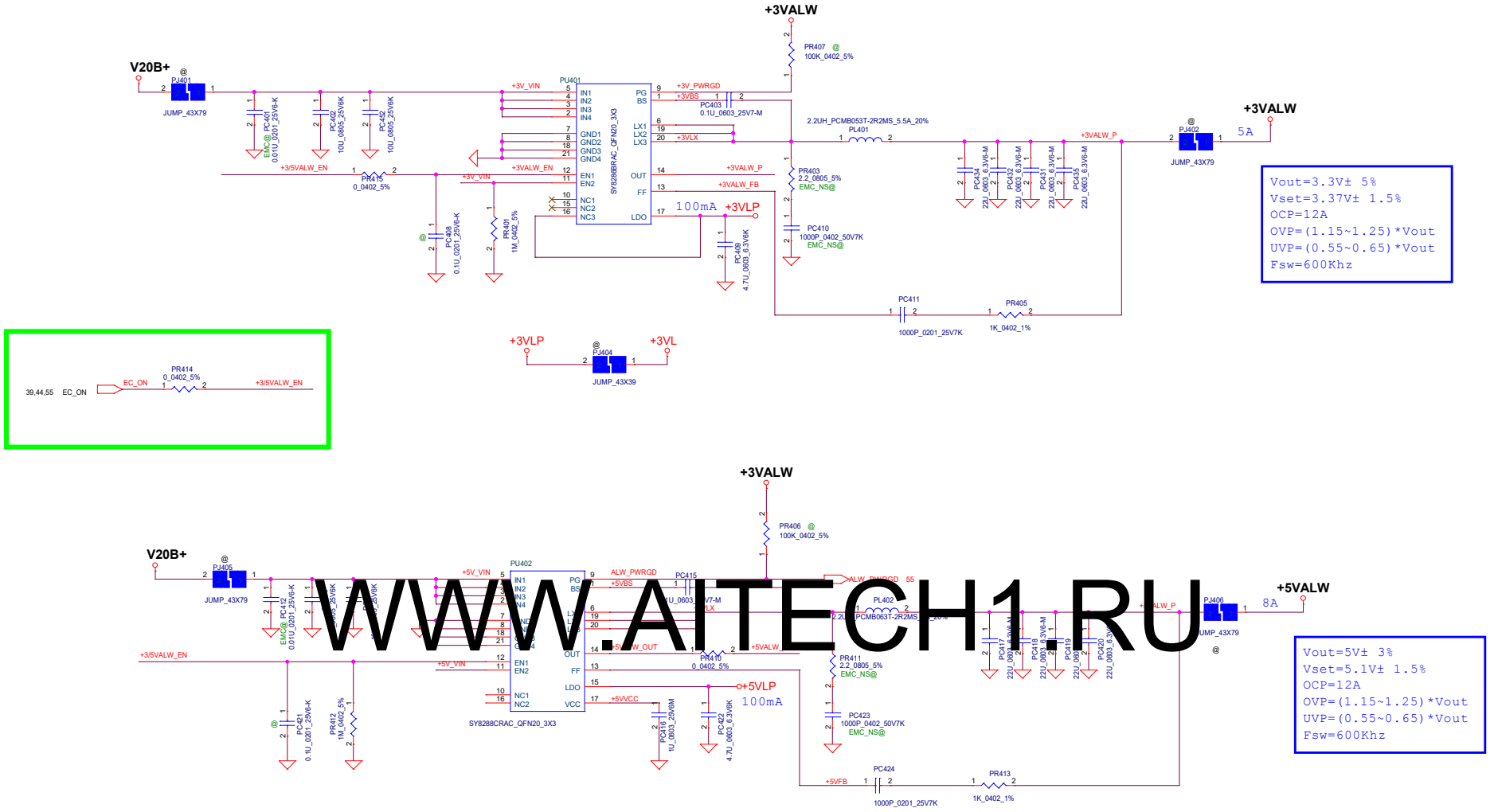

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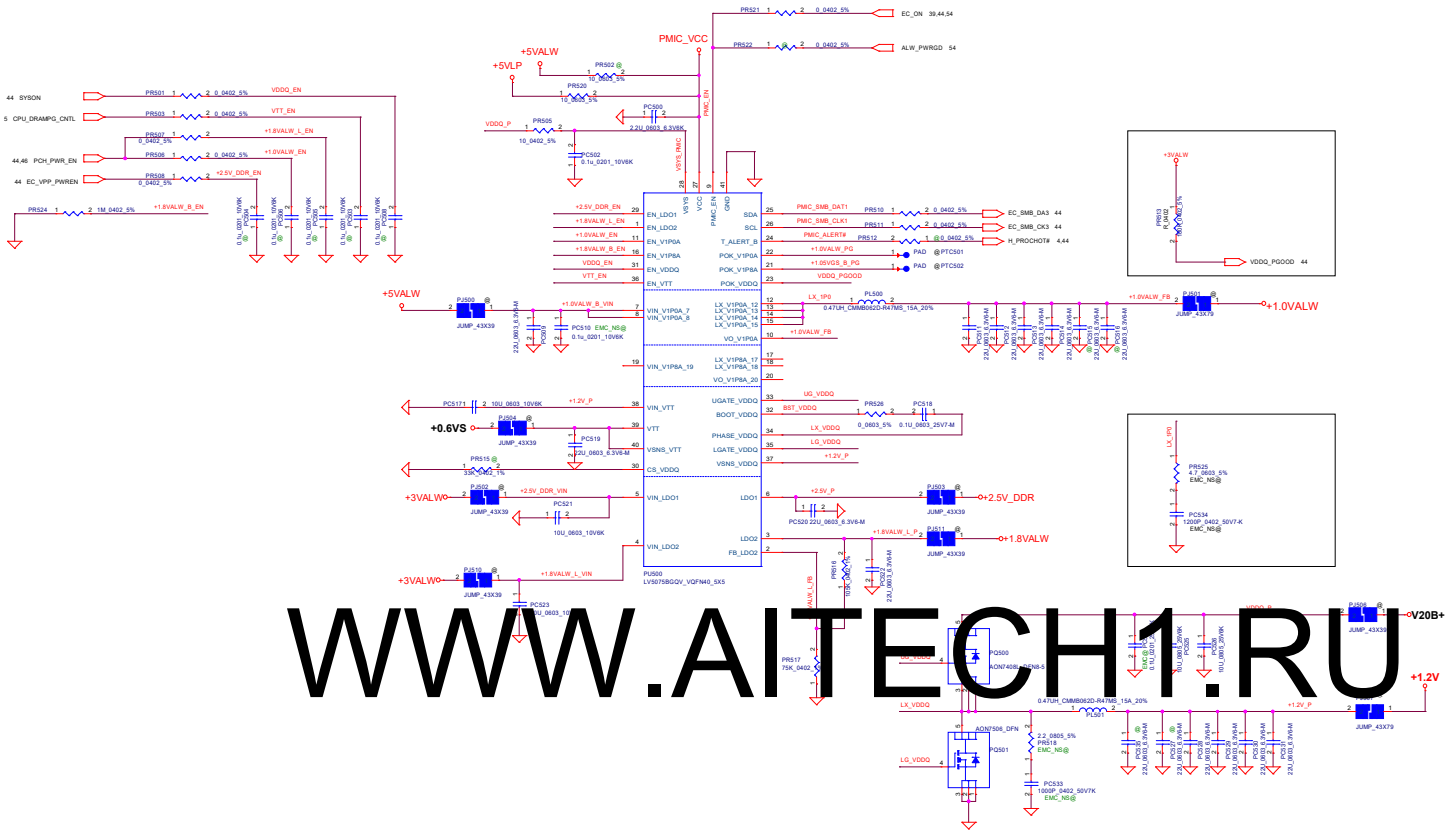
Title	PWR_3VALW/5VALW		
Size	Document Number		Rev
C	DG42A		0.1
Date:	Thursday, May 04, 2017	Sheet	54 of 60


PMIC_VCC
+5VALW
+5VLP
+0.6VS
+3VALW
+2.5V_DDR
+1.8VALW
+1.0VALW
+1.2V
V20B+
PU500
LV5075BGQV_VQFN40_5X5
PG500
PG501
PL500
PL501
PL502
PJ500
PJ501
PJ502
PJ503
PJ504
PJ505
PJ511
PJ512
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Title

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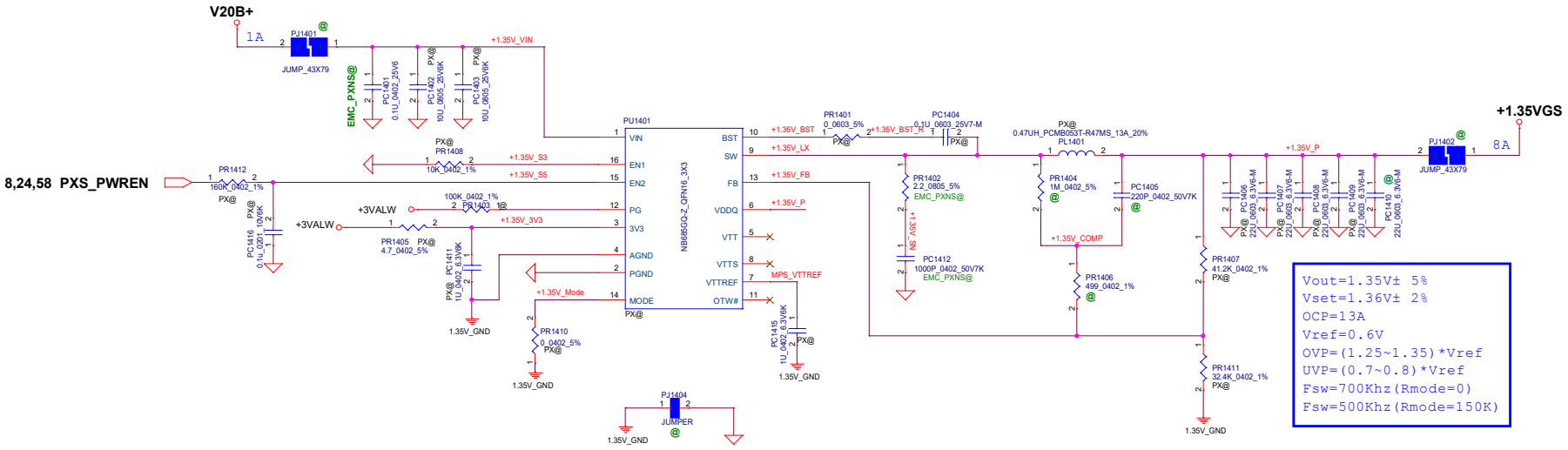

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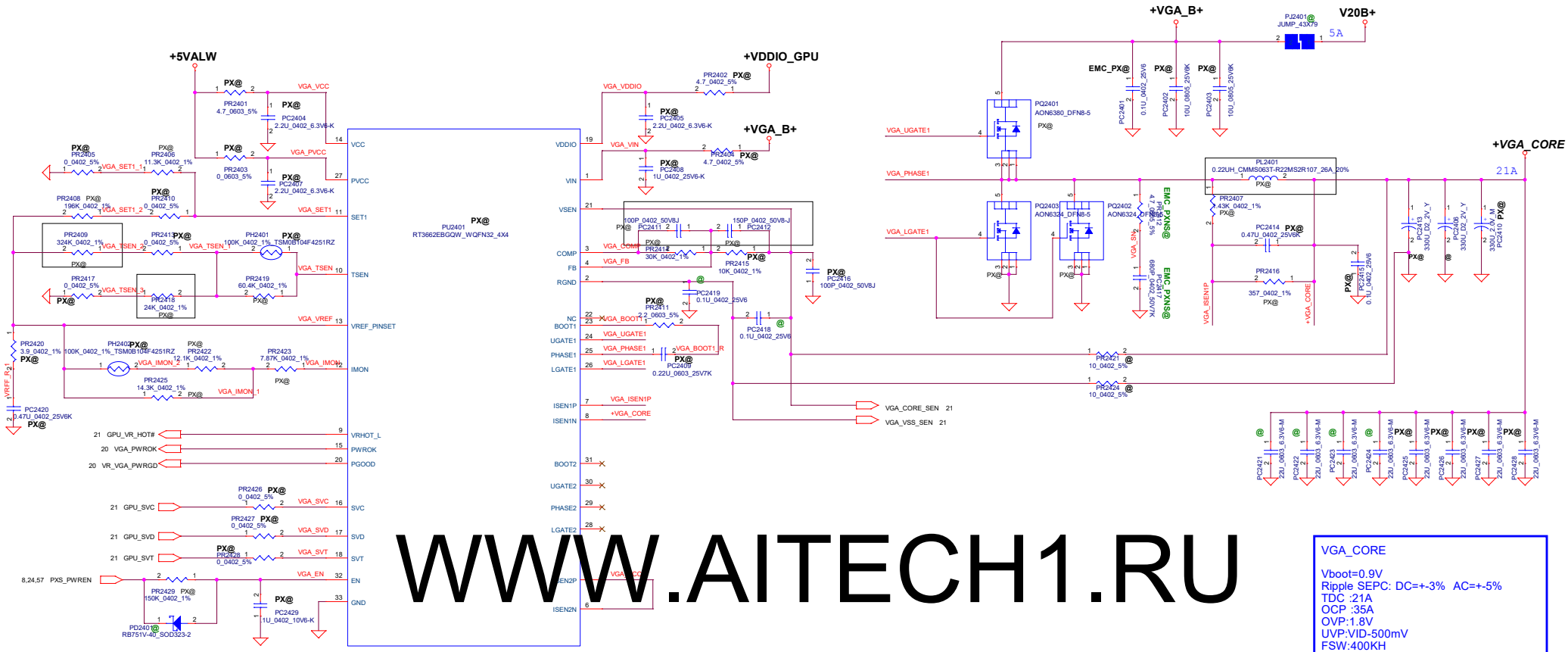
Title	PWR-+1.05VGS/+1.35V_VRAM		
Size	Document Number		Rev
C	DG42A		0.1
Date:	Thursday, May 04, 2017	Sheet	57 of 60



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VGA_CORE

Vboot=0.9V
Ripple SEPC: DC=+-3% AC=+-5%
TDC :21A
OCP :35A
OVP:1.8V
UVP:VID-500mV
FSW:400KH

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Issued Date	2016/08/16	Deciphered Date	2017/08/15

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Title: PWR-VGA_CORE_AMD

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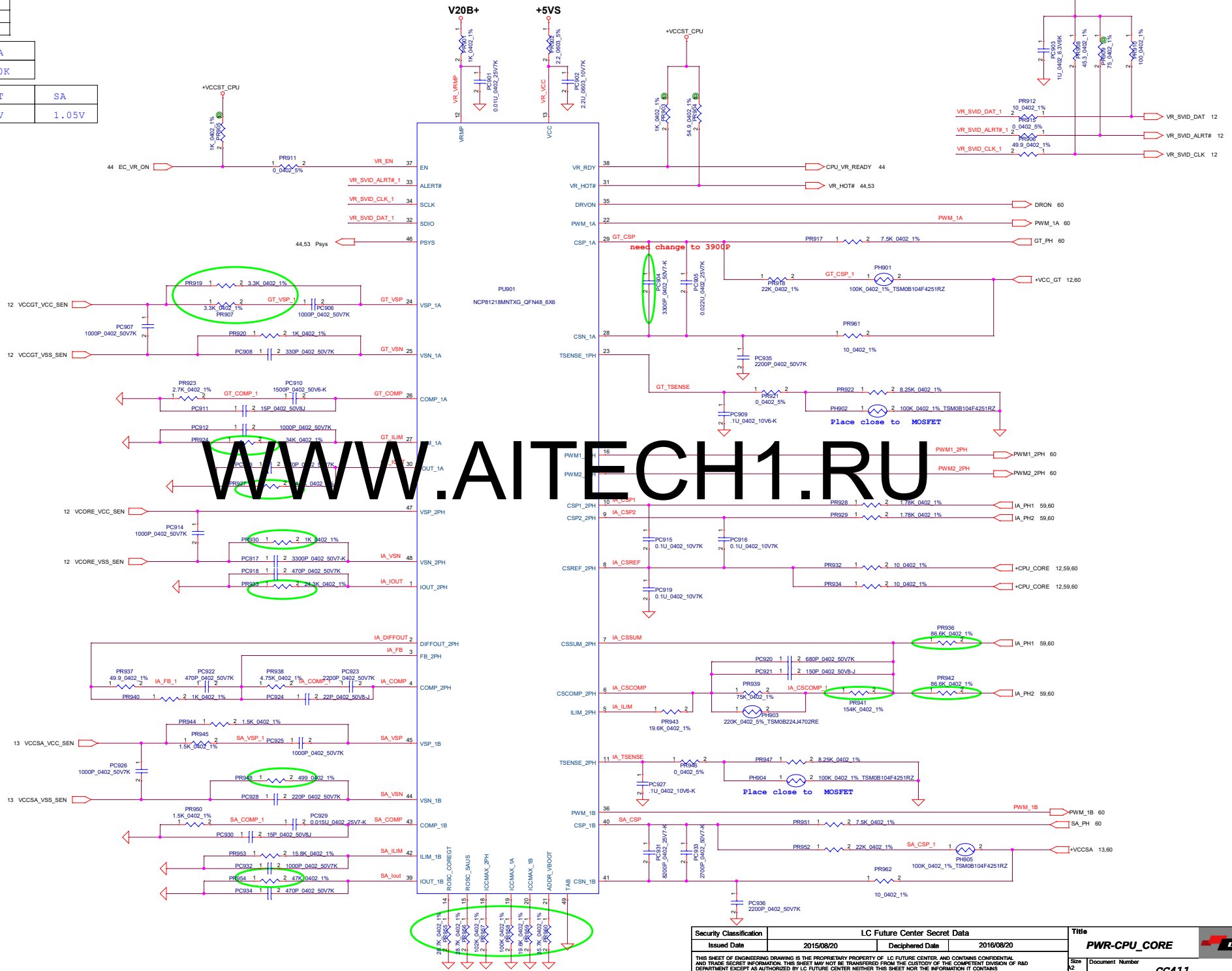
SVID Specification	
	Config
Vmin(V)	0
Vmax(V)	1.52
Vstep(mV)	5

RFsw	Core/GT	SA
28.7K	550K	550K

RVboot	Core	GT	SA
35.7K	0V	0V	1.05V



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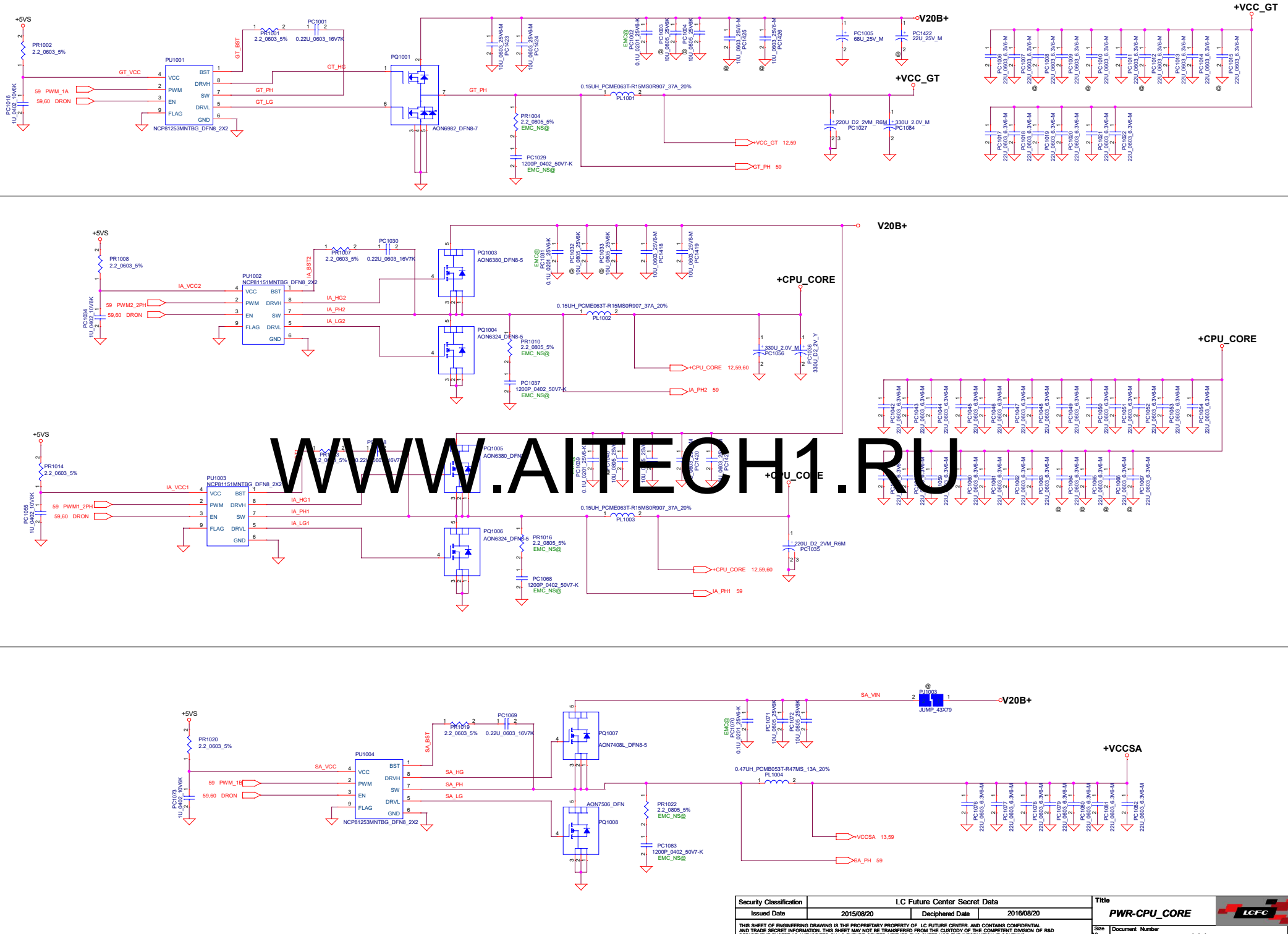

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Title: PWR-CPU_CORE

Size	Document Number	Rev
A2	CG411	0.1

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